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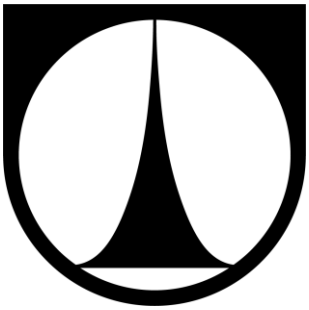

DIPLOMA THESIS

DEVELOPMENT OF ELECTRICAL TESTS FOR AN ELECTRONIC BOARD

ENTWICKLUNG VON ELEKTRISCHEN TESTS FÜR EINE ELEKTRONISCHE LEITER-PLATTE

NÁVRH ELEKTRONICKÉHO TESTERU PRO TEST ELEKTRONICKÝCH DESEK

Bc. JAN KAZDA

Leader:	prof. Dr.-Ing. Dietmar Scharf	Zittau, 2014
Consultant:	Dipl.-Ing. Claus-Uwe Bönicke	Riesa, 2014

Technical University of Liberec
Faculty of Mechatronics, Informatics and Interdisciplinary Studies
Academic year: **2013/2014**

DIPLOMA THESIS ASSIGNMENT

(PROJECT, ART WORK, ART PERFORMANCE)

First name and surname:	**Bc. Jan Kazda**
Study program:	**N2612 Electrical Engineering and Informatics**
Identification number:	**M11000291**
Specialization:	**Mechatronics**
Topic name:	**Development of electrical tests for an electronic board**
Assigning department:	**Institute of Information Technology and Electronics**

Rules for elaboration:

1. Analysis of the circuit and investigation of functionality of assembled components.
2. Splitting up the test requirements into individual test steps.
3. Cost estimating of the test.
4. Development of test software.
5. Construction of adapters, creating of additional resources for test.
6. Document the test and the details of the test equipment with the focus is on quickly scan for errors on Device-Under-Test.
7. Debugging of test sections.
8. Creating documents for production schedule.

Scope of graphic works:	**Dle potřeby dokumentace**
Scope of work report (scope of dissertation):	**cca 40 - 50 stran**
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[1] **SPRINT 4510 AFTS: PRACTICAL INNOVATIONS IN FLYING PROBE TEST TECHNOLOGY. In: Acculogic Inc.: SPRINT 4510 AFTS [online].**

[2] **GENRAD. Introduction to GR228X Test Systems. USA, 1999**

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BuS Elektronik GmbH & Co. KG

Diploma thesis

Specialist study: Electrical science
Student:
Personal-Number:

Company's coach: Certificated engineer Claus-Uwe Boenicke

Contents of the project

- Development of electrical tests for an electronic board.
- Tests have to be economical and must look at following single tasks:

- Analysis of the circuit and investigation of functionality of assembled components.
- Splitting up the test requirements into individual test steps.
- Cost estimating of the test.
- Development of test software.
- Construction of adapters, creating of additional resources for test.
- Document the test and the details of the test equipment with the focus is on quickly scan for errors on Device-Under-Test.
- Debugging of test sections.
- Creating documents for production schedule.

12.2.2014

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Assignment for the master thesis

Course of studies: EMIm11, St.-Nr: 204 903 // Liberec, Mechatronics, M11000291

Student's name: Jan Kazda

Subject: DEVELOPMENT OF ELECTRICAL TESTS FOR AN ELECTRONIC BOARD

Assignment:

Tests have to be economical and must look at following single tasks:

- Analysis of the circuit and investigation of functionality of assembled components.
- Splitting up the test requirements into individual test steps.
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- Construction of adapters, creating of additional resources for test.
- Document the test and the details of test equipment with the focus is on quickly scan for errors on Device-Under-Test.
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Dean

Declaration

Byl jsem seznámen s tím, že na mou diplomovou práci se plně vztahuje zákon č. 121/2000 o právu autorském, zejména § 60 (školní dílo).

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Diplomovou práci jsem vypracoval samostatně s použitím uvedené literatury a na základě konzultací s vedoucím diplomové práce a konzultantem.

V Riese dne:

Acknowledgements

I would like to thank all, who helped me make my diploma thesis, especially to my consultant in the company Bus Elektronik, GmbH & Co. KG, Mr. Dipl.-Ing. Claus-Uwe Boenicke, who lead me through all challenges in my diploma thesis and gave me helpful hints of practical use. Next main acknowledgement is for my leader, prof. Dr.-Ing. Dietmar Scharf, for supervising my diploma thesis.

Next I would like to thank my family who has supported me all through my time of studying and during the time I wrote my diploma thesis.

And at the end I would like to thanks to company BuS Elektronik, GmbH & Co. KG in Riesa, Germany, represent by its owner, Mr. Dr. Maiwald for providing me the diploma thesis and for all services for the time of working on my diploma thesis.

Anotace

Diplomová práce je zaměřena na návrh a výrobu testovacího adaptéru a software pro otestování funkčnosti jednotlivých částí již osazených desek plošných spojů (DPS, PCB).

Cílem práce je vytvoření přípravku pro otestování elektronické funkcionality (ICT) jistého daného vzorku série DPS, na kterém bude posléze otestována celá tato série. Dále je cílem práce vytvoření obslužného programu pro daný tester a testovací system, který automaticky, či poloautomaticky proměří jednotlivé osazené součástky na desce plošných spojů a zjistí, zdali jsou funkční či nikoli a zdali mají správnou hodnotu v daných tolerancích.

Dále bude práce obsahovat další části, které budou sloužit pouze k ilustraci řešení obdobných problémů jinými metodami, či řešit tématiku blízkou danému tématu, se kterou je v praxi úzce spojen.

Veškerá měření a syntaxe programů budou prováděny v system GenRad™, pod který spadá i mnou použité testovací pracoviště GX228X, pro které budou programy tvořeny a na kterém budou posléze i odladěny.

Tato práce bude vykonávána pod záštitou firmy BuS Elektronik GmbH & Co. KG se sídlem v Riese, kde bude také tato diplomová práce řešena.

Klíčová slova:

PCB, DPS, Test DPS, GenRad™, ICT, GX228X, elektronické součástky, deska plošných spojů, osazování DPS, nefunkční DPS, elektronický test, funkční test, kalkulace, BuS Elektronik GmbH & Co. KG

Abstract

The diploma thesis is aimed at design and production of testing module and software development for testing the functionality of each part of an already assembled PCB.

The goal of this work is to develop a device for testing electronic functionality of certain given sample of series PCB. At this device will be following testing of whole series. The next goal of my work is to develop the utility software for given tester and testing system. This will automatically or self-automatically measure each assembled component on PCB and find out if the component is working and it is in the right tolerance of the given value.

In addition, this diploma thesis contains sections for also illustrating how similar problems can be handled alternatively as well as describing practical examples thematically linked close together.

All measuring and program syntax will be made for the system GenRad™. Part of this system is the testing workplace GX228X at which I will work. For this workplace will be development all programs and debugged after development.

This work will be done under the auspices of company BuS Elektronik GmbH & Co. KG with headquarters in Riesa, where my diploma work will takes place.

Keywords:

PCB, DPS, testing of DPS, GenRad™, ICT, GX228X, electronic components, printed circuit board, assembling of PCB, broken PCB, electronic test, functionality test, calculation, BuS Elektronik GmbH & Co. KG

Anmerkung

Die Diplomarbeit ist auf die Entwicklung und Herstellung von Test-Modul und Software zum Testen der Funktionalität jedes Teil bereits bestückter Leiterplatte gerichtet.

Das Ziel dieser Arbeit ist es, ein Gerät zum Testen von elektronischer Funktionalität bestimmter, gegebenerMuster einer Serie von PCB zu entwickeln. An diesem Tester wird der Test der ganze Serie folgen. Das nächste Ziel meiner Arbeit ist es, die Utility-Software für bestimmte Tester und Testsystem zu entwickeln. Dadurch wird automatisch oder selbst automatisch jede bestückte Komponente auf dem PCB gemessen und getestet, ob die Komponente funktioniert undihr Wert in den richtigen Toleranzen liegt.

Des Weiterenenthält die Diplomarbeit Abschnitte, die nur für die Illustration des Umgangs mit ähnlichen Problemen durch andere Methoden dienen, oder beschreibt thematisch eng mit diesem verbundene praktische Beispiele.

Alle Messungen und Programm-Syntax werden im Rahmen des Systems GenRad™ vorgenommen. Unter dieses System fällt der GR228x Arbeitsplatz, an dem ich arbeiten werde. Für diesen Arbeitsplatz werden alle Programme entwickelt und eingemessen.

Diese Arbeit steht unter der Schirmherrschaft der Firma BuS Elektronik GmbH & Co. KG mit Sitz in Riesa, wo meine Diplomarbeit realisiert und geschrieben wird.

Keywords:

PCB, DPS, Prüfung von DPS, GenRad™, ICT, GR228x, elektronische Bauteile, Leiterplatten-Montage von PCB, PCB gebrochen, elektronischer Test, Funktionstest, Berechnung, BuS Elektronik GmbH & Co. KG

Contents

List of used symbols and shortcuts

U	V	voltage
I	A	current
R	Ω	resistor
C	F	capacitor
L	H	inductor/coil
mili	m	x 10^{-3}
mikro	*μ*	x 10^{-6}
nano	n	x 10^{-9}
piko	p	x 10^{-12}
kilo	k	x 10^{3}
mega	M	x 10^{6}
ω	rad/s	angular velocity
π		Ludolphian number (= 3,141 592 653 …)

DC	Direct current
AC	Alternating current
PCB, DPS	Printed Circuit Board
CAD	Computer-aided Design
IC, U	Integrated circuit
Q	Transistor
X	Connector
W	Transformer

ICT	Circuit Description file extension
TPX	Test Program file extension (contains temporary nails)
TPG	Test Program file extension (contains permanent nails)
ERR	Circuit Description Error File file extension

LIS	Fixture Translation Listing File file extension
IDX	In-circuit Diagnostic Data File file extension (contains temporary nails)
IDD	In-circuit Diagnostic Data File file extension (contains permanent nails)
NCL	Nail Contact List File file extension
NDB	Nail Database File file extension
OBC	Object Code File file extension
SMT	Symbol Table File file extension
ATP	Analog Test Program File file extension
VLSI	Very Large Scale Integration
DUT	Device Under Test
Fig. #	Figure № #
Code #	Program Code № #
Tab. #	Table № #
Supp. #	Supplement № #

1. Introduction

The testing of Printed Circuit Boards (PCBs) is necessary for the correct functioning of the product. For a single produce or low-volume- with only passive parts we can test the board manually, using only multi-meters, oscilloscope, voltage and current source and tester's knowledge. But this is not possible in hi-volume production, where in most cases processors, memories and other complicated parts are included, which can't be measured by such simple means. Therefore test equipment, which not only testing the whole board to make sure it is electrically working and correct, but also its functionality too. This happens in one measurement and takes far shorter time than if it would be processed manually.

Possible testing methods are different in the aim of the using. Most common tests are the electronic test and the optical inspection test. The further information will be described below.

I have divided my work into two parts. The first part will be the main theme of my diploma thesis, which focuses on work with the PCB tester for given printed circuit board. This will contain the whole process of construction since the schematic plan to the final equipment works in production.

The second part will illustrate the process of calculation at testing before the beginning of development, as the answer for customer price request.

Fig. 1 Automated line of PCB assembling and testing [10]

Even though here are the fully automated lines for assembling, soldering and testing PCBs (*Fig. 1*), in small series or complicated boards is more economically and easy to make the external tester which can test the board well and it can be modify every time if it is necessary. And this will be our case. To produce the external tester for testing small series of boards, which are not economical to test on the automatic line.

2. Theoretical part

2.1. About PCB

2.1.1. History

Development of the methods used in modern printed circuit boards started early in the 20th century. In 1903, a German inventor, Albert Hanson, described flat foil conductors laminated to an insulating board, in multiple layers. Thomas Edison experimented with chemical methods of plating conductors onto linen paper in 1904. Arthur Berry in 1913 patented a print-and-etch method in Britain, and in the United States Max Schoop obtained a patent to flame-spray metal onto a board through a patterned mask. Charles Durcase in 1927 patented a method of electroplating circuit patterns.

The Austrian engineer Paul Eisler invented the printed circuit while working in England around 1936 as part of a radio set. Around 1943 the USA began to use the technology on a large scale to make proximity fuses for use in World War II. After the war, in 1948, the USA released the invention for commercial use. Printed circuits did not become commonplace in consumer electronics until the mid-1950s, after the Auto-Sembly process was developed by the United States Army.

Before printed circuits (and for a while after their invention), point-to-point construction was used. For prototypes, or small production runs, wire wrap or turret board can be more efficient. Predating the printed circuit invention, and similar in spirit, was John Sargrove's 1936–1947 Electronic Circuit Making Equipment (ECME) which

sprayed metal onto a Bakelite plastic board. The ECME could produce 3 radios per minute.

During World War II, the development of the anti-aircraft proximity fuse required an electronic circuit that could withstand being fired from a gun, and could be produced in quantity. The Centralab Division of Globe Union submitted a proposal which met the requirements: a ceramic plate would be screenprinted with metallic paint for conductors and carbon material for resistors, with ceramic disc capacitors and subminiature vacuum tubes soldered in place. The technique proved viable, and the resulting patent on the process, which was classified by the U.S. Army, was assigned to Globe Union. It was not until 1984 that the Institute of Electrical and Electronics Engineers (IEEE) awarded Mr. Harry W. Rubinstein, the former head of Globe Union's Centralab Division, its coveted Cledo Brunetti Award for early key contributions to the development of printed components and conductors on a common insulating substrate. As well, Mr. Rubinstein was honored in 1984 by his alma mater, the University of Wisconsin-Madison, for his innovations in the technology of printed electronic circuits and the fabrication of capacitors.

Originally, every electronic component had wire leads, and the PCB had holes drilled for each wire of each component. The components' leads were then passed through the holes and soldered to the PCB trace. This method of assembly is called through-hole construction. In 1949, Moe Abramson and Stanislaus F. Danko of the United States Army Signal Corps developed the Auto-Sembly process in which component leads were inserted into a copper foil interconnection pattern and dip soldered. The patent they obtained in 1956 was assigned to the U.S. Army. With the development of board lamination and etching techniques, this concept evolved into the standard printed circuit board fabrication process in use today. Soldering could be done automatically by passing the board over a ripple, or wave, of molten solder in a wave-soldering machine. However, the wires and holes are wasteful since drilling holes is expensive and the protruding wires are merely cut off.

From the 1980s small surface mount parts have been used increasingly instead of through-hole components; this has led to smaller boards for a given functionality and lower production costs, but with some additional difficulty in servicing faulty boards. [7]

2.2. Testing PCB

Testing of DPS can be dividing into more parts by the position of production in what they are. The determining aim is if the boards are assembled or not, because both tests are particularly different. In the describing I will aimed to the boards after assembling, because it is that what I will do in my work.

This main difference can be subdivided into two more main parts, as was sad in introduction (*Chap. 1*). At the electronic test (ICT) of each component at PBC if it is possible of course and at the functionally test (FCT) and at optical inspection (AOI). The electronically test testing if the each component has the right value and if it works well. This test is based on measurement of basic electric values like as current, voltage, resistance, capacitance and inductance. With combination of these we can measure every component.

2.2.1. Testing of unassembled boards

2.2.1.1. Bare-board test

Bare board testing involves using capacitance and resistance tests. Capacitance testing for a bare board (*Fig. 2*) involves testing for opens and shorts by "charging" a net or plane and then probing each net to measure the induced capacity. Inaccuracies occur with this method because of the inherent variability in producing circuit boards. However field measurement or field effect testing for shorts uses a very similar approach. [8]

A bed of nails tester (*Fig. 2, Supp. XXIII*, *Supp. XXXVII*) is a traditional electronic and bare-board test fixture which has numerous pins inserted into holes in an Epoxy phenolic glass cloth laminated sheet (G-10) which are aligned using tooling pins (*Fig. 3*) to make contact with test points on a printed circuit board and are also connected to a measuring unit by wires (*Supp. XXIV*). Named by analogy with a real-world bed of nails, these devices contain an array of small, spring-loaded pogo pins; each pogo pin makes contact with one node in the circuitry and so tested the continuity and non-shorted nets on the PCB (by the data generated from the Gerber or CAD data). [13]

For this testing we have many shapes of nails, which can be used for different cases. From the normal cone shape via the pyramid shape to the special nails with isolation for special use. Some of the available shapes we can see at the picture hereinafter (*Fig. 3*).

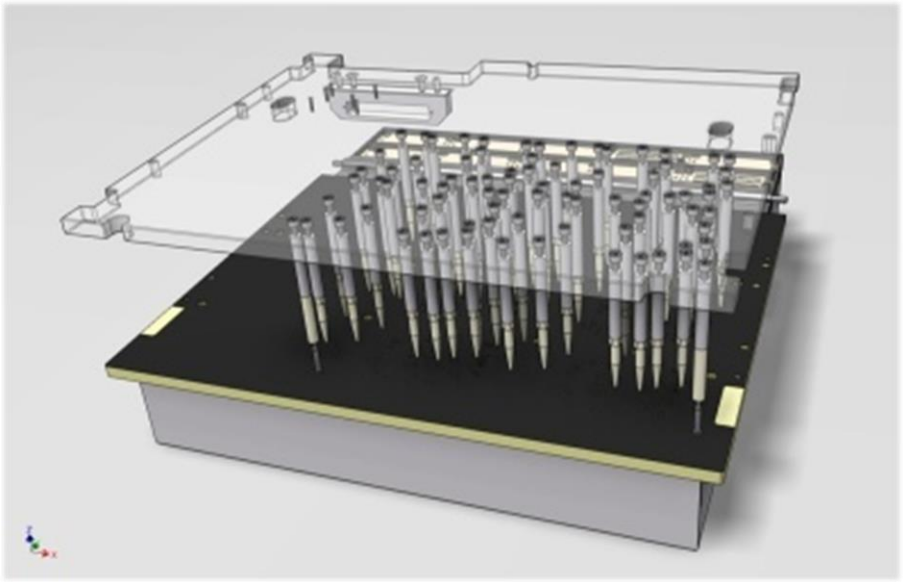

Fig. 2 Bed of nail for bare-board test and ICT [20]

2.2.2. Testing of assembled boards

2.2.2.1. Electronic testing

2.2.2.1.1. Inter Circuit Test (*ICT*)

In-circuit testing methods are used to check for manufacturing faults. Manufacturing faults are defects in individual components and inter-connections on the board. To test components individually, connections from the test system to all functioning component pins (*Fig. 3*) is required.

This is accomplished using a test fixture (*Fig. 2*) that mates with each of the board's circuit nodes and test methods that can effectively isolate a single component from the parts surrounding it. An in-circuit component test is often performed as the first or second test after a board has been assembled and soldered. It may be preceded by a separate bare board test (*Chap. 2.2.1.1*) to check for opens and shorts in the conductive tracks before parts are inserted.

In-circuit tests generally fall into four test categories:

- Connectivity tests that check for shorts and open connections on the board
- Analog tests that measure component values
- Digital tests that check the operation of digital integrated circuits
- Hybrid tests that check components that are a combination of analog and digital components

The System contains test hardware appropriate for each kind of test, but it must be connected to each part on the board individually before you can perform a test. Since components are tested individually, the system can usually localize a fault immediately and issue a report telling the operator or technician which part needs repair. Interactive faults that can cause the board to malfunction are generally overlooked, but such faults are rare on a well–designed board.

Fig. 3 Available testing nails and itself shapes

The in-circuit tests are generated by the Automatic Test Generation (*ATG*) software (*Fig. 16*). Programmers who need to modify tests created by *ATG* or who need to write tests of their own should thoroughly understand these techniques and the criteria *ATG* uses in selecting various test methods.

The most troublesome aspect of the in-circuit test is the assumption that you can test each component as if it were the only part on the board. Fairly complex test strategies are often required to analyze the component's circuit environment and to

isolate the component from the surrounding circuits. Since these test strategies involve only individual components and their immediate circuit connections, you can assemble libraries of standard test procedures and adapt them to the limited range of environments in which the components are found. Given an appropriately coded description of the circuit, the system software can write the entire board test by drawing tests for individual components from test libraries. *VLSI* devices are tested in a way that is, in principle, no more complex than the method used for simple components. [5]

While in-circuit test is a very powerful tool for testing PCBs, it has these limitations:

- Parallel components can only be tested as one component if the component is same, but different component in parallel connection sometimes can be tested for each component in different testing method
- Electrolytic components can be tested for polarity only on specific configuration (e.g. if not parallel connected to power rails) or with specific sensor
- The quality of electrical contacts cannot be tested
- It is only as good as the design of the PCB. If no test access has been provided by the PCB designer then some tests will not be possible. [13]

By pressing the DUT down against the bed of nails, reliable contact can be quickly and simultaneously made with hundreds or even thousands of individual test points within the circuitry of the DUT (*Supp. XLI*). The hold-down force may be provided manually or by means of a vacuum, thus pulling the DUT downwards onto the nails.

Devices that have been tested on a bed of nails tester may show evidence of this after the fact: small dimples (from the sharp tips of the Pogo pins) can often be seen on many of the soldered connections of the PCB.

Typically, four to six weeks are needed for the manufacture and programming of such a fixture. Fixtures can either be vacuum or press-down. Vacuum fixtures give better signal reading versus the press-down type. On the other hand, vacuum fixtures are expensive because of their high manufacturing complexity. The bed of nails or fixture as generally termed is used together with an *ICT* tester.

This technique of testing PCB's is being slowly superseded by boundary scan (*Chap. 2.2.2.1.4*) techniques (silicon test nails), automated optical inspection, and built-in self-test, due to shrinking product sizes and lack of space on PCB's for test pads. [13]

2.2.2.1.2. Flying probe test

These systems are often used for only testing basic production, prototypes, and boards that present accessibility problems. Flying probe testing uses electro-mechanically controlled probes to access components on printed circuit assemblies (PCAs) (*Fig. 4*). Commonly used for test of analog components, analog signature analysis, and short/open circuits. They can be classified as in-circuit test (*ICT*) systems or as Manufacturing Defects Analyzers (MDAs). They provide an alternative to the bed-of-nails technique for contacting the components on printed circuit boards. The precision movement can probe points on PLCCs, SOICs, PGAs, SSOPs, QFPs and others, without any expensive fixturing or programming required.

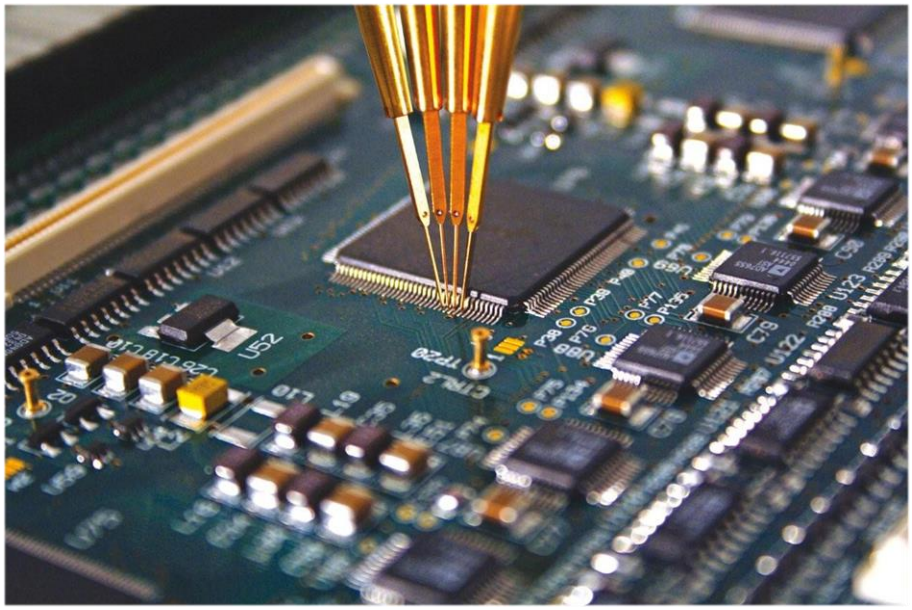

Fig. 4 Flying probe tester in work [19]

Benefits are lower cost than Bed Of Nails (*Chap. 2.2.1.1*, *Fig. 2*), because no fixturing required and fast time to first test, because of fast development cycle. [16]

2.2.2.1.3. Functional circuit test (*FCT*)

The functional circuit test is typically performed in the last phase of the production line of a product, as a final quality control. *FCT* are performed to ensure that the device under test (DUT) fulfills its functional specifications.

FCT consists in emulating or simulating the operational environment of the product in order to check its correct functionality. The environment includes, as an example, any device that communicates with the DUT, the power supply of the DUT, loads necessary to make the DUT work properly. [14]

To connect the device under test (DUT) to the test instruments, you must construct a fixture that mates easily with the board and provides reliable electrical connections. Usually, you only need to test the board's inputs and outputs, and the fixture needs to provide little more than the board's normal interface connectors. Therefore, the test fixture (*Fig. 5*) can be relatively simple and inexpensive to construct, which is especially attractive for low–volume testing. Using a functional tester, it is often possible to test a variety of bus–oriented boards from an edge connector in a single fixture.

With power applied to the board, a functional test checks that the board, or chosen sections of the board, produces the desired output response when various input stimuli are applied. Functional testing can also check that further stages of assembly have not damaged the board.

When a board fails a functional test, the test cannot always identify the cause of the fault immediately since there can be any number of paths from the inputs to the outputs along which the fault might lie. As boards become more complex, the possible signal paths become much longer, and the simple information that a particular board output has failed becomes less useful in identifying the cause of the failure. After a board fails a functional test, a technician usually has to trace the fault from the output back to its origin. [5]

Test software is the one that allows production line operators perform the functional test in an automatic way through a computer. To do this, the software communicates with external programmable instruments as Digital MultiMeter, I/O boards, communication ports, etc.

Fig. 5 Functionally fixture for assembled board [22]

The software in conjunction with the test fixture that interfaces the instruments with the DUT, make possible to perform a FCT. [14]

2.2.2.1.4. Boundary scan (*BS*)

Method for testing interconnects (wire lines) on printed circuit boards or sub-blocks inside an integrated circuit. Boundary scan is also widely used as a debugging method to watch integrated circuit pin states, measure voltage, or analyze sub-blocks inside an integrated circuit.

The Joint Test Action Group (JTAG) developed a specification for boundary scan testing that was standardized in 1990 as the IEEE Std. 1149.1-1990. In 1994, a supplement that contains a description of the Boundary Scan Description Language (BSDL) was added which describes the boundary-scan logic content of IEEE Std. 1149.1 compliant devices. Since then, this standard has been adopted by electronic device companies all over the world. Boundary scan is now mostly synonymous with JTAG.

The boundary scan architecture provides a means to test interconnects (including clusters of logic, memories, etc.) without using physical test probes; this involves the addition of at least one test cell that is connected to each pin of the device and that can selectively override the functionality of that pin. Each test cell may be programmed via the JTAG scan chain to drive a signal onto a pin and thus across an indi-

vidual trace on the board; the cell at the destination of the board trace can then be read, verifying that the board trace properly connects the two pins. If the trace is shorted to another signal or if the trace is open, the correct signal value does not show up at the destination pin, indicating a fault.

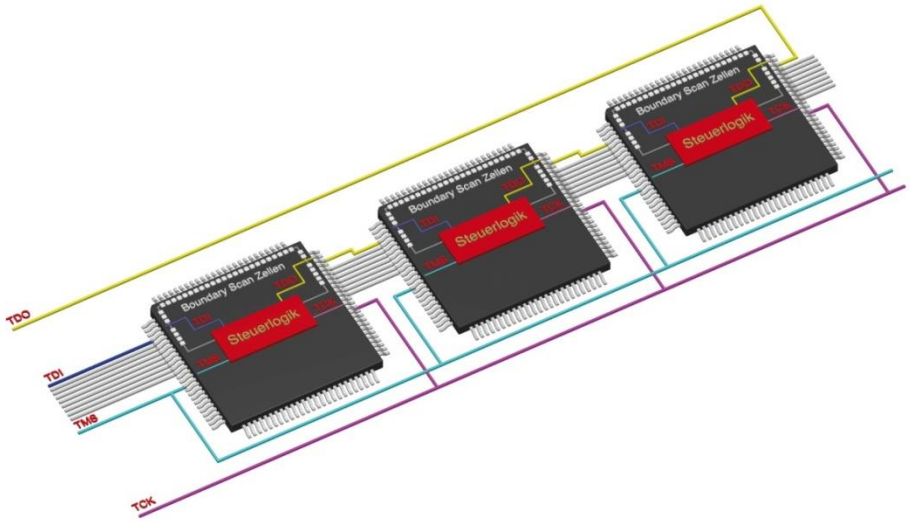

Fig. 6 Illustration of idea of boundary scan [21]

As the cells can be used to force data into the board, they can set up test conditions. The relevant states can then be fed back into the test system by clocking the data word back so that it can be analyzed (*Fig. 6*).

By adopting this technique, it is possible for a test system to gain test access to a board. As most of today's boards are very densely populated with components and tracks, it is very difficult for test systems to physically access the relevant areas of the board to enable them to test the board. Boundary scan makes access possible without always needing physical probes. [15]

2.2.2.2. Optical testing

The test methods described in following two subchapters can be used for the testing of unassembled board too (*Chap. 2.2.1*). But in most cases are used just for the testing of assembled boards as control of right position and well soldering and particularly can be used for the test of right value/type if is printed on the case of that component.

2.2.2.2.1. Automatic Optical Inspection (*AOI*)

An automated visual inspection of a wide range of products, such as printed circuit boards (PCBs), LCDs, transistors, lids and labels on product packages or agricultural products (seed corn or fruits). In case of PCB-inspection, a camera autonomously scans the device under test (DUT) for variety of surface feature defects such as scratches and stains, open circuits, short circuits, thinning of the solder as well as missing components, incorrect components, and incorrectly placed components. Agricultural inspections might check for variations in part color, perhaps to find ripe fruit. AOI is a type of white box testing. It is commonly used in the manufacturing process because it is a non-contact test method. AOI is able to perform most of the visual checks performed previously by manual operators, and far more swiftly and accurately. AOI systems are implemented at many stages through the manufacturing process. They are used for inspecting parts that have limited and known variations. For defect or flaw detection, the AOI system looks for differences from a perfect part. There are systems capable of bare board inspection, solder paste inspection (SPI), as well as inspecting the component placement prior to reflow, the post-reflow component conditions, and post-reflow solder joints. These inspection devices all have some common attributes that affect capability, accuracy, and reliability.

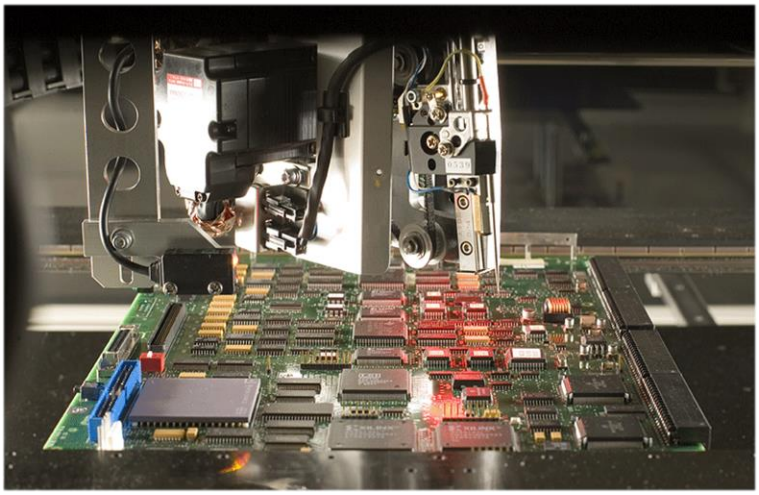

Fig. 7 AOI - Automatic Optical Inspection [11]

In this way AOI can be used to detect problems early in the production process. Since faults cost more to fix later in the production process, it is essential to notice problems early. For example, problems in the solder and assembly area of a PCB can be seen early in the production process and information used to feedback quickly to previous stages, avoiding the production of too many boards with the same problem.

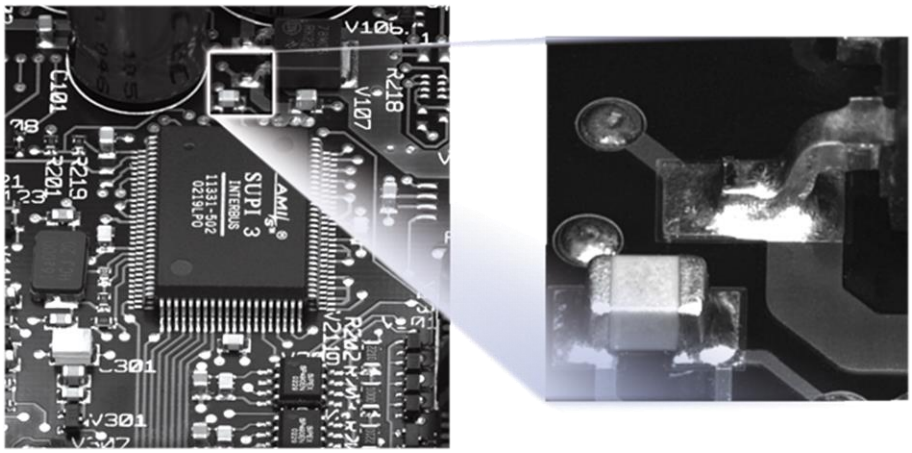

Fig. 8 Scene from optical inspection of PCB [9]

Low costs and programming efforts make AOI a practical and powerful quality tool for both prototypes and high-volume assembles. It is often paired with the testing provided by boundary scan test, in-circuit test, x-ray test, and functional test. In many cases, smaller circuit board designs are driving up the demand for AOI versus in-circuit test. [12]

2.2.2.2.2. CT (X-ray) scan test

With the complexity of circuit boards increasing and size decreasing, it is becoming more and more difficult to measure and examine the component features inside. Traditionally analysis using 2D X-ray is performed on circuit board components to inspect the internal parts. Industrial computed tomography (CT) scanning can check inside the circuit board components in 3D for failure or a defect. CT scanning is a non-contact inspection test which creates a 3D rendering from over 1300 2D X-ray slices. Not only is industrial CT scanning used for visual purposes but even metrology is possible, therefore measurement is possible.

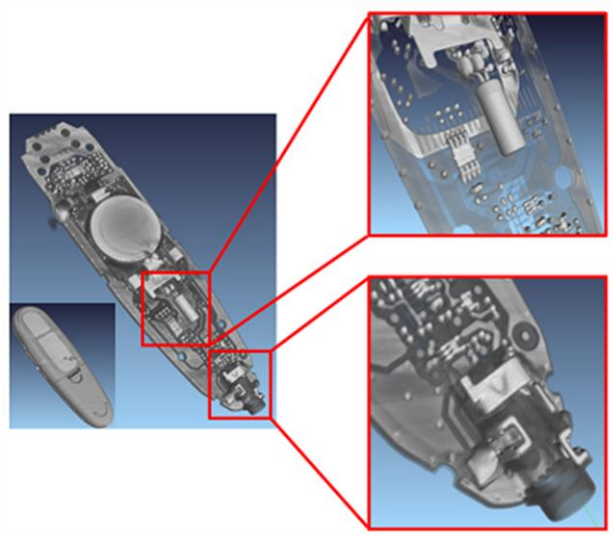

Fig. 9 Example of using CT in electronic test of assembled device [18]

2.3. Used method in my diploma thesis

In this case I will use only the ICT test (*Chap. 2.2.2.1.1*), because the function test was not ordered by the customer and the customer does not specify any parameters for the functionality test and the dummy test was not necessary, because of the absence of any logic circuit. This is chose to because in the department where I work there have been designs for the bed of nails fixtures for electronic and functional testing. Because of this fact, I describe this method more than the others.

The machine which will be used in this company are from the firma GenRad™ (in 2002 GenRad™ was bought by Teradyne). More about these machines will be located in the following subchapter (*Chap. 2.3.1*).

2.3.1. Short introduction of test system GR228X

The machines are different in how much pin their multiplexor can master. The main differences between each type are summarizing hereinafter (*Tab. 1*). Here we can see that the main differences are between the counts of maximal available nails for testing.

Table 2–1
GR228X System Configurations

System Type	Pin Board (Type)	Pin Boards (Max)	Driver/ Sensors per board	Avail. Nails (Max)	Mux Ratio	Data Rate
GR2280	Combo I	10 [1]	16	1280 [2]	2:16	5 MHz
GR2281	Combo II	10 [1]	32	1280 [2]	2:8	5 MHz
GR2281A	ASM [3]	11	0	1408	2:8	Not Applicable
GR2282 [4]	Combo I	30	16	3840	2:16	5 MHz
GR2283 [5]	Combo I	15	16	1920	2:16	5 MHz
GR2284 [5]	Combo II	15	32	1920	2:8	5 MHz
GR2285e	XP [6]	15	32	1920	2:8	10 MHz
GR2286 [4]	Combo I	30	16	3840	2:16	5 MHz
GR2286 [5]	Combo I	30	16	3840	2:16	5 MHz
GR2287 [4]	Combo II	30	32	3840	2:8	5 MHz
GR2287 [5]	Combo II	30	32	3840	2:8	5 MHz
GR2287L [7]	HDC1	30	32	7680	2:16	5 MHz
GR2287LX [7]	HDC2	30	64	7680	2:8	5 MHz
GR2287A	ASM [3]	30	0	3840	2:8	Not Applicable
GR2288 [4]	Combo II	9	32	1152	2:8	5 MHz
GR2289e	XP [6]	30	32	3840	2:8	10 MHz

[1] System allows 11 pin boards if the AFTM is not installed.
[2] 1408 if 11 pin boards are present
[3] Analog Scanner Modules
[4] Windows NT PC Retrofitted system
[5] *e*-Series system or *i*-Series system
[6] Xtended Performance
[7] High Density Card 1. You must have a minimum of two HDC1s. Optionally, you can populate the GR2287L with up to 28 Combo II pin boards.
[7] High Density Card 2. You can only populate the GR2287LX with HDC2 pin boards.

Tab. 1 GR228X System configurations [5]

From these testers I will work with GR2281 (*Fig. 10*) which is satisfied my requests to test my board.

The GR2281 Production Test Systems are designed to provide comprehensive testing for small to large scale Printed Circuit Boards (PCB) and assemblies. Each Production Test System provides full analog and digital measurement capabilities for testing.

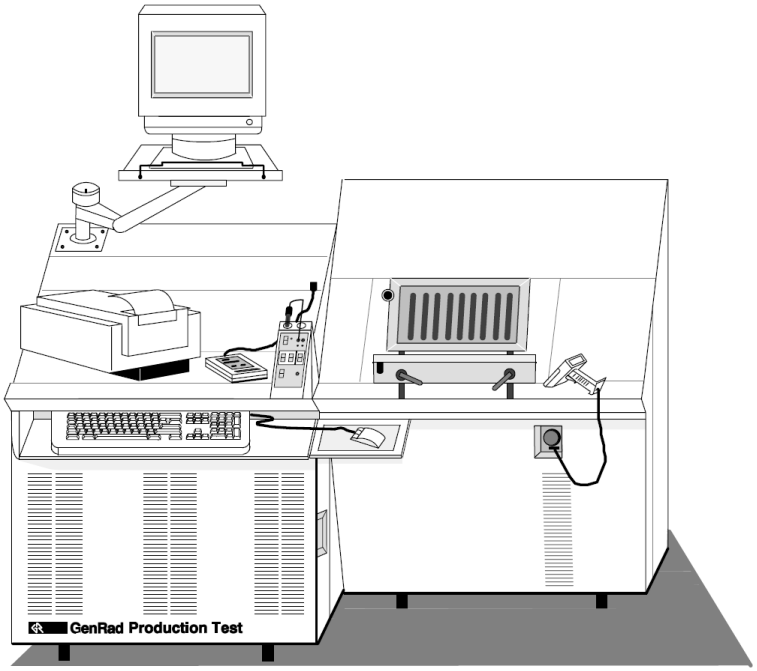

Fig. 10 Used testing machine GenRad™ GR2281 [5]

In addition, some functional tests can be performed with the standard system measurement modules. External measurement or source devices, controlled via an IEEE bus interface option, can be added to expand the functional test capabilities. These external instruments can be connected to the system's scanner subsystem through the external multiplexer ports.

A unique test program and test fixture, called a test set, must be developed for each type of board to be tested. The test program contains many individual in-circuit component tests. These tests are usually created by the system's Automatic Test Generator (*ATG*) (*Fig. 16*) software, which is part of the test system's program preparation software.

In the following pictures (*Fig. 11* and *Fig. 12*) from the tester manual [5] are illustrations of the steps, which are necessary to do in the process of development and

testing of one each PCB. The first step is to collect all materials and information which are necessary for successfully creating and testing the circuit on PCB. The next step is to make a *CKT* file (*Chap. 3.1.4*) either manually from the Bill Of Material (BOM), or automatically from CAD data. With this data we can generate the test program (*ATG*) and the files which will be created in this process (*Chap. 3.1.5*). Mainly they are *TPX*, *ERR* and other. When the TPX file is translated successfully, we can make a Nail Assignment (*Chap 3.1.6*, *Fig. 17*). This process will change the name of pins. With all of these steps we can make the fixture (*Chap. 3.1.10*) as it illustrated in the fifth step of graph.

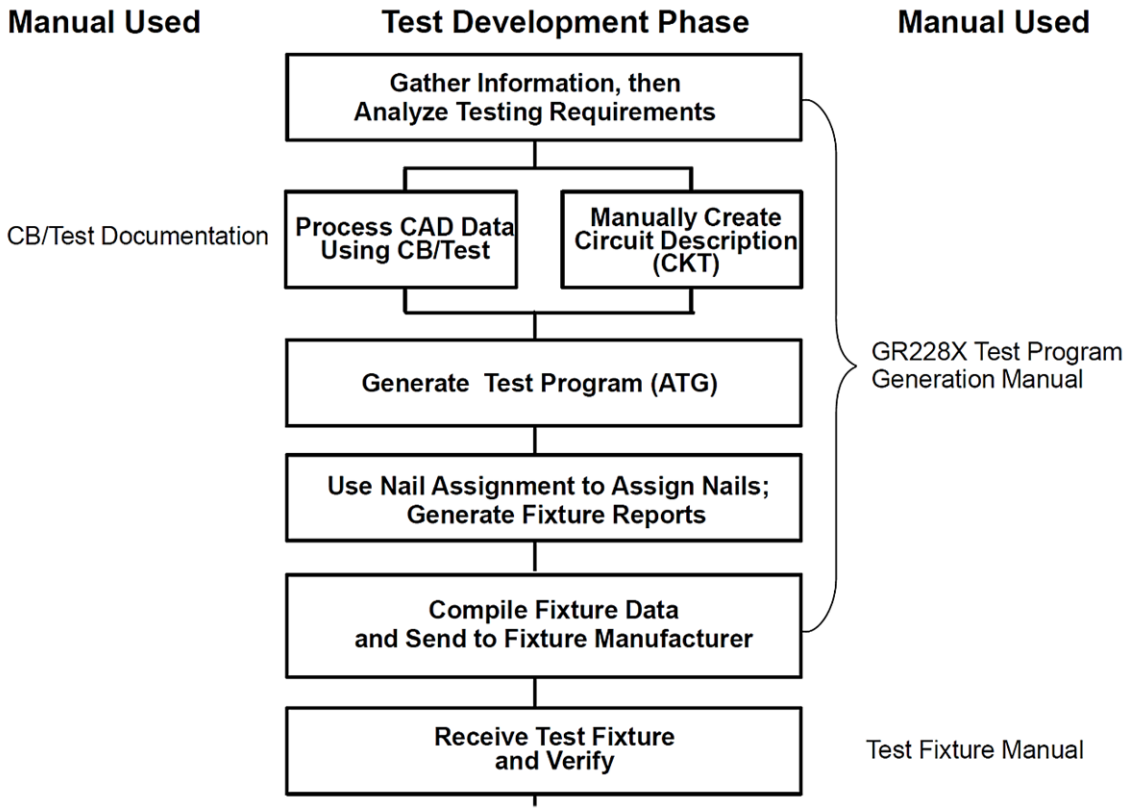

Fig. 11 Test Development Phase – part 1

Until the fixture is completed, we can jump over the sixth step and translate the Test Program File (*Chap. 3.1.7*, *Fig. 19*). While the fixture is completed we can continue in the process of debugging our program with the board in the fixture (*Chap. 3.1.11*). At the same time of the debugging of the program, it is good to update the Test Program (*TPG*). At the end, after the steps are passed, we can release the fixture with the program to production as it is shown in the last step.

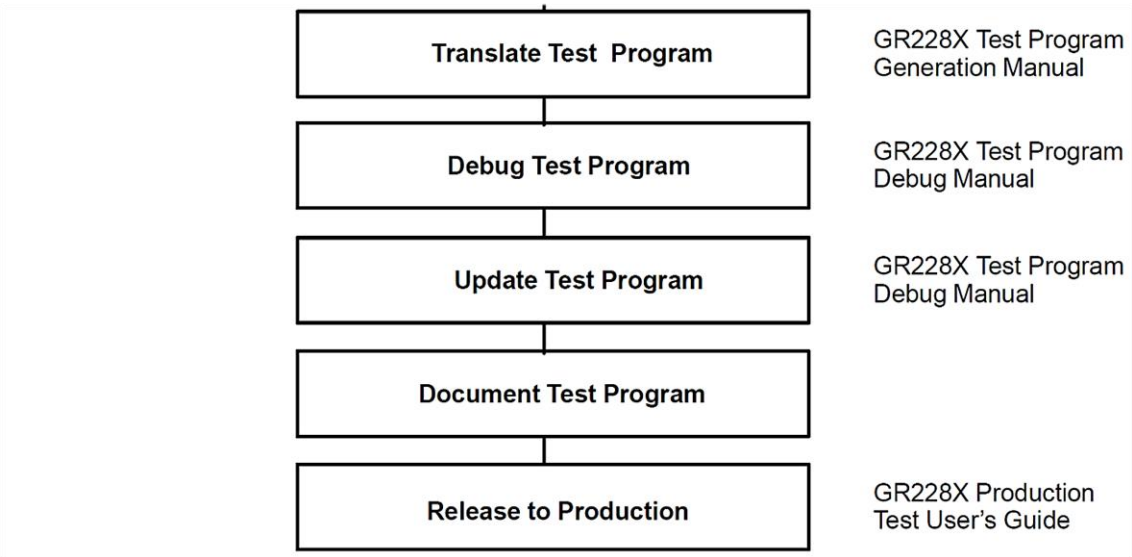

Fig. 12 Test Development Phase – part 2

2.3.1.1. Basic methods using for automatic measuring by GR228X

This system uses an inner multiplexor for applying the voltage/current sources and measurement equipment. This means every component is connected to the two or more nails by which is measured through the multiplexors (*Supp. V*). In a normal case we can use only two channels of multiplexor for measurement (in case of two-port network; in case of multi-ports the count of pins higher). But in many cases we need more than two wires, because the component could be branched around by other components, which are necessary grounded and guarded or we simply need to use more measuring equipment, which cannot be connected onto one nail, e.g. Kelvin's method. This is better described above (*Chap. 3.1.7*, *Fig. 21*).

2.3.1.1.1. Resistance measurement

The measuring of resistance is done by applying the voltage to the component and measures the flowing current through the component. The final resistance is calculated by using the Ohm law which is shown thereinafter (*2.1*).

$$R = \frac{U}{I} \quad [\Omega] \tag{2.1}$$

The voltage limit is default set to the value 200mV and the current limit is set up to the 128mA, which means the minimal resistance of 1,563Ω. For the smaller value can be used the 4-wires Kelvin method.

2.3.1.1.2. Capacitance measurement

The capacitance is measured similar to the impedance measurement, where we want to know the impedance Z_C (*2.2*). From this value and from the known frequency we can get the right value of capacitor.

$$Z_C = \frac{1}{2\pi f C} = \frac{1}{\omega C} \quad [\Omega] \tag{2.2}$$

From the equation above we get the equation for calculation of capacitance (*2.3*).

$$C = \frac{1}{2\pi f Z_C} = \frac{1}{\omega Z_C} \quad [F] \tag{2.3}$$

The default voltage limit is set to 200mV or 1V and the frequency is set to 1kHz or 10kHz.

2.3.1.1.3. Inductance measurement

The inductance measurement is similar, like as the Capacitance measurement, but only the measured value and the equation for calculating the final value are different. The equation for calculating the impedance of the coils is hereinafter (*2.4*).

$$Z_L = 2\pi f L = \omega L \quad [\Omega] \tag{2.4}$$

After simple alteration we can get from the equation above to the final expression for calculating the inductance value (*2.5*)

$$L = \frac{Z_L}{2\pi f} = \frac{Z_L}{\omega} \quad [H] \tag{2.5}$$

Default values given by the GenRad™ system are the voltage value of 200mV or 1V and the frequency limits of 100Hz, 1kHz or 10kHz.

2.3.1.1.4. Diode measurement

The test of normal diodes is done in the forward direction. The diode is connected to a low voltage source with current limit, e.g. 2,1V @ 10mA and the voltage at the cross of the diode should be measured. Usually it is about 0,7V, which is the threshold voltage of most used silicon rectifying diodes. For other materials or types of diode the threshold voltage can be different, e.g. for germanium it is about 0,2V but LED diodes should be about 1,8V or more in dependence of light spectrum, luminosity, color and power.

In the case of measurement of LED diodes we cannot find out the color by this manner, so that must be done by a visual inspection from operator.

2.3.1.1.5. Zener diode measurement

The measurement of the Zener diodes is quite similar to the normal diode test. The difference is in the polarity of the testing diode. In this case it is in the reverse direction. Next to it, is a higher voltage at the source. It should be a few volts higher than the Zener voltage of the diode. The current is limited up to 20mA, but can be decreased by adding the serial resistor, but the voltage of the source must be increased

in dependence at used resistor. Next will be the voltage measured on the diode, our required Zener voltage.

Usable range of Zener voltage is wide from 1,2V up to 200V. [24]

2.3.1.1.6. Amplifying factor of bipolar transistor

The easiest way how to test functionality of the transistor is to measure itself, amplifying factor β. This says in simplicity how much bigger the current is flowing through the collector than it is flowing through the base (*2.6*). In literature there is this factor marked by more symbols. But the most common is exactly β, h_{FE} (FE means Forward Emitter) or h_{21e} (index 21 is derived from the 2nd and 1st quadrant of VA characteristics of bipolar transistor).

$$\beta = h_{FE} = h_{21e} = \frac{(I_{E2} - I_{E1}) - (I_{B2} - I_{B1})}{I_{B2} - I_{B1}} = \frac{i_E - i_B}{i_B} \qquad (2.6)$$

Describing of the equations (*2.6*) above is simple. The small letters of currents means the dynamic parameters. That means, for example, we made two measurements and the small i_x will be the difference between two measured values, or ΔI_x, where *x* marks the index of current.

In practice looks the measurement follow. At the collector, the connected voltage source with constant voltage output is continuous. Then the base is connected to the current source with a known constant current I_{B1} for each measurement. When the current flows through the transistor, we can measure the current in emitter I_{E1}. After measuring we change the value of the current flowing to the base I_{B2} and measure the emitter current I_{E2} again. From these values we can calculate the amplifying factor by using the equation above (*2.6*).

2.4. About calculation

Calculation is one of the components of the so-called management accountancy. By calculation we understand the allocation of costs per cost unit.

Cost unit is the elementary unit of power, e.g. 1pcs, 1 kg, 1 hour, etc. – that such an entity for which it makes sense to find out the costs. Calculation shows how costs were or will be incurred to production of one such cost unit.

Calculation is basically divided into two main groups: (which are next divided into other subgroups) – the preliminary calculation and final calculation. As the name suggests, the preliminary calculation is determined from before, up to the beginning of production. We can base it on e.g. consumption standards and standards efforts from historical experience and estimates, budgets indirect (overhead) costs, etc. The main objective of the preliminary calculation is to determine how costs will be incurred at the origin (production) of the cost per unit and whether, therefore not e.g. a product is worth producing.

The final calculation is contrary compiles at the end of the production task and indicates the actual costs incurred through making per the calculation unit. Basis for the final calculation is primarily provided by the internal accounting and production records.

The final and the preliminary cost is used, among other tools for the pricing calculation unit (product).

In the calculation we distinguish direct and indirect (overhead) costs:

- Direct costs are directly identifiable per the cost unit such as the consumption of materials or wages. The preliminary estimate is based on the calculation of these costs, mainly from the above-mentioned material consumption standards or standards effort.
- Indirect or overhead costs are common to the production of all goods or more broadly for the whole company. These include the costs of energy consumption, depreciation of fixed assets, payroll overhead staff (heads of production), but also the pay of the administrative apparatus of the company. These costs are not usually directly attributable to the cost

unit and because it is used with a variety of methods, such as simple calculation by dividing, overhead rate calculations or calculations with evaluative numbers. The preliminary calculation of overhead is usually based on budget overhead.

It is customary to prepare the calculation by using the calculation formula, which is actually a series of individual cost items. For the existence of Czechoslovakia there was a "federal" Decree on the calculation, which also indicated a standardized calculation formula. Nowadays it is up to each company to determine the calculation formula itself.

Possible calculation formula might look like this:

1) Raw material (material immediately necessary for production)
2) Direct wages (wages of workers producing of the product)
3) Manufacturing overhead (overhead = common costs of production)
4) Σ(1-3): OWN COSTS OF PRODUCTION
5) Administrative expenses (common costs for the administrative apparatus)
6) Supply arrangement (common supply costs for the company)
7) Σ(4 +5 +6): OWN COST PERFORMANCE
8) Distribution costs / overheads (related to consumptions - sales)
9) Σ(7 +8): FULL CUSTOM PERFORMANCE COSTS

The whole cost of production actually reports all expenses that a company incurred or will incur at manufactured cost per unit. The cost of final production is also influenced by the final selling price - the company would probably not have to sell their products (cost unit) for a price lower than the full cost of their own for a long time – they would be selling for a loss. [23]

2.5. Uses of calculation

After making the pre-calculation, it is then sent to the customer for verifying the price of the order. If the customer is satisfied with the preliminary price the order can follow. After ordering there will be work at the DPS begin. In the first case the customer must supply all materials and documents which are necessary for the production, i.e. schematic drawing, the design of PCB, if the customer have it, the BOM (Bill Of Material) for ordering the components from supplier and for using it in designing of test software, casing, and other documents if they are any. When we have completed the production of the order, i.e. assembled the PCB and tested it, we can then make the final calculation and final price of order. This one can be quite different than the pre-order price offer. But it should not be different so much, because we are taking a risk that the order will not be sold by the customer. If there will be any problems or complications which will increase the price of the order, it is a necessity to consult this problem with the customer and to confirm that he will accept the price change.

Next is the pre-calculation necessary for the intercompany accounting and economy, because we need to know if the company will be prosperous or if it will be operating at a loss. It is also important to decide if the company will use its own capital to fund the order.

3. Practical part

3.1. DC/DC converter

3.1.1. Preparations of documents

Before beginning the work, it is necessary to collect all documents about my project. This means the documents, which I will need to develop my fixture and following measurement. In the initial schematic circuit plans created by the customer (*Supp. I*, *Supp. II*, *Supp. III* and *Supp. IV*), the complete CAD design of PCB from the PCB department or from the customer if the customer has the design). These are two main things which we will need for our work. The next document is the Bill Of Material (BOM) which is necessary for making of the *CKT* file. With these three documents I can start my work and do it successfully. The next useful document can be the required test methods from the customer – if he wants to make only electronic tests (ICT) or full testing – electronic and functional (ICT + FCT) or if he wants any special order for marking after tested for example.

In my case I get the schematic circuit from the customer, CAD design of PCB is designed by a different department in the company and the BOM plus the request for making the ICT test.

3.1.2. Methodic of numbering the connections

The first step of constructing the fixture for any board is to number the nets. This is because the tester works with the multiplexer and each component must be measurable between two or more multiplex inputs and to every net must be assigned its number.

If we have, in the schematic circuit, the points for testing included, we number it by its number. But the test points must not be everywhere in the circuit, so we must control the possibility that every component could be tested. If we find that there aren't any nets without marked test points, we can mark it more. But we must be thinking of the fact, that every number must be unique for the whole circuit!

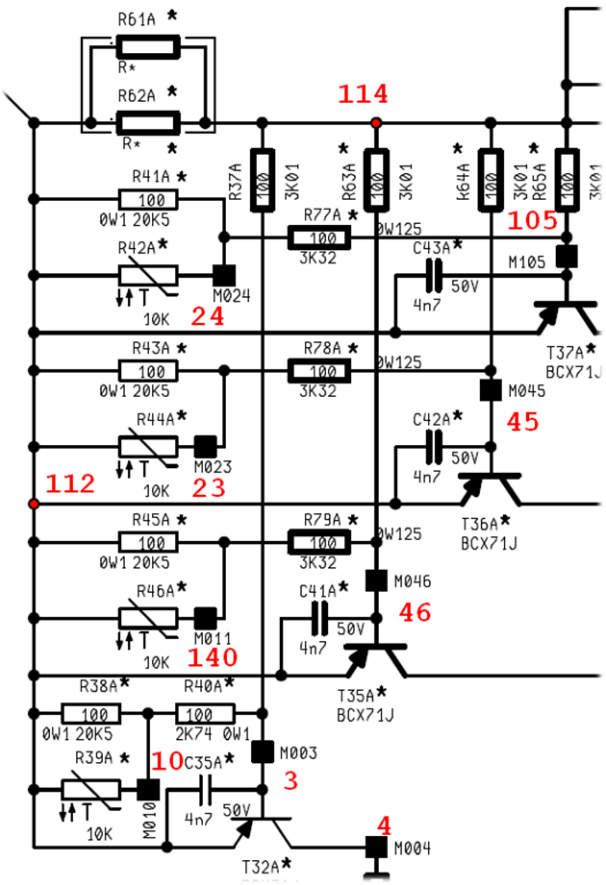

Fig. 13 Numbering of test points at schematic circuit

In the picture above (*Fig. 13*) we can see the example of numbering in our scheme. The marked test points are in circuit numbered by code M plus three incremental numbers. The added point is, for example the pin number 114 or 112. The meaning of the colored highlight is described in one of next chapters (*Chap. 3.1.12*).

Here can be the case that we have only a few test points at the schematic circuit from the customer and the use of other points for testing the PCB is prohibited. In this case we must use only these points and in the next step must tune the measuring software.

3.1.3. Methodic of numbering connections on PCB

After we have completed the numbering of lines on the printed schematic circuit on the paper, we can start with numbering the points in CAD file with complete

PCB. This is harder than numbering on the schematic circuit, because here we must find the right net in the tangle of other nets. The work is facilitated by the tool which is included in CAM350 and which is called *Query Nets*. This tool highlights the net which is selected between other. After highlighting the net we can see the connections between components and can precisly decide what is this net at the schematic circuit and place on it the test point and its number.

In the CAD file extra points can be placed, especially for testing and it is a priority to use them. In another way, we can use the pads of components contact.

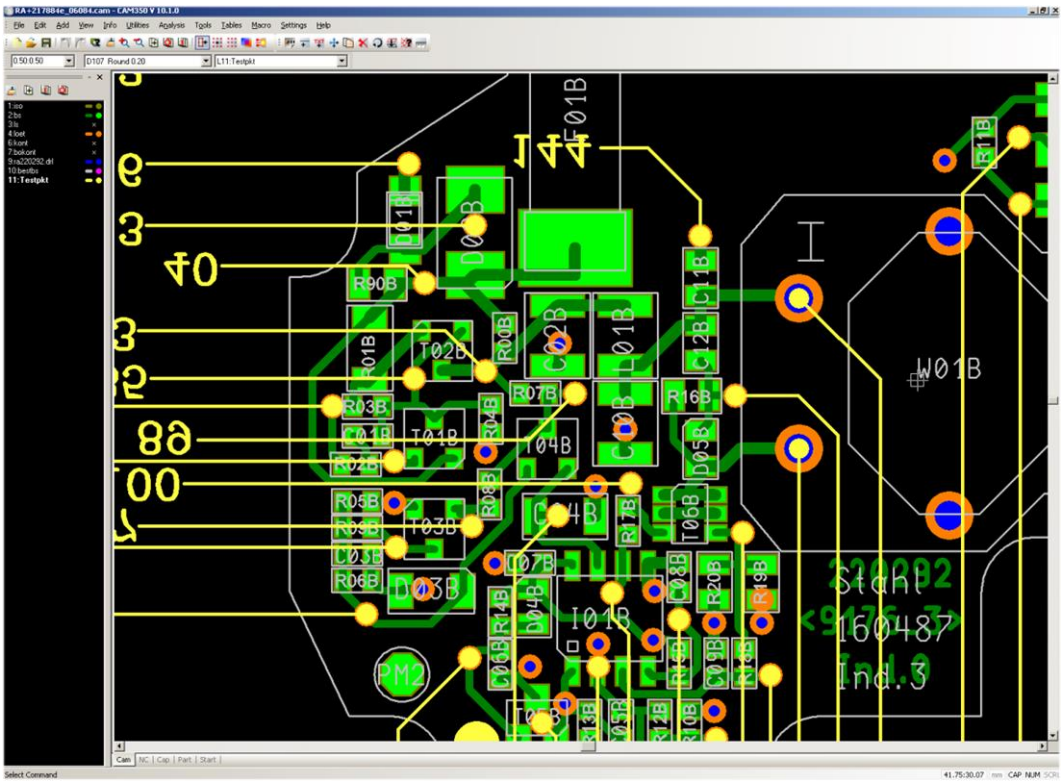

Fig. 14 Placing test points into CAD file

The numbering itself is done in the new layer called *Testpkt* because of clarity (*Fig. 14, Supp. VI*). The dimensions of the test flash, line and number are given by intercompany non-writing rules. The dimension of test flash is in code D139 which means rounded shape with diameter of 1,02mm. The lines has size code D106, which means diameter of 0,18mm and the numbers dimensions are from 2,00mm to 2,30mm height and by size code of lines D107 which means 0,20mm wide line.

Next we must take a look at the dimensions between two flashes. The minimal allowed dimension is 1,8mm center to center, because of electric security and mechanical performance.

This layer will be used for the development of the fixture and drilling and wiring the nails, so we must take care to the clarity of numbering and layering. The non-write rule is to respect the rule of not crossing lines between numbers and flash each other. The numbers should be placed outside of the shape of the board, but it is not a rule. If it is possible to add the number inside the board, we can place it there.

Once the numbering is finished, we get the map (*Fig. 15*,*Supp. VIII*) of test points, which will be placed on the bottom side (wiring side) of the fixture.

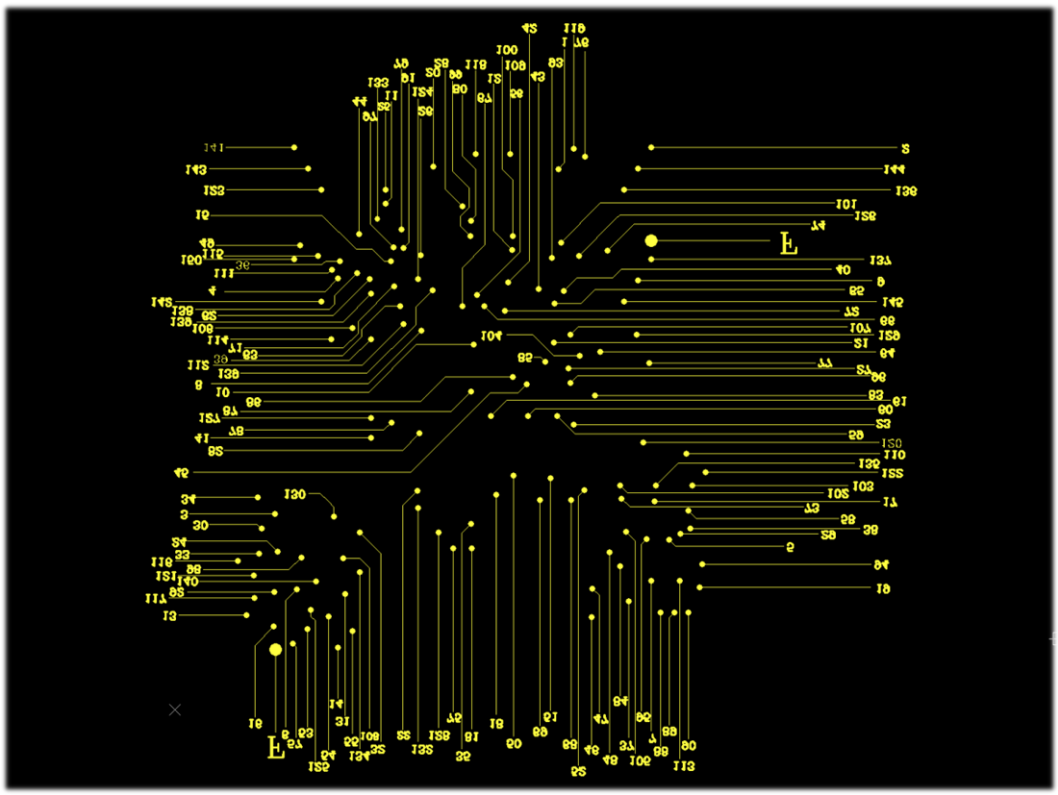

Fig. 15 Map of test points (with temporary numbering)

The letters ***F*** on the test points map (*Fig. 15, Supp. VIII*) means, that here will be the fixture nails for the centering of the board on the fixture above the test nails.

3.1.4. *CKT* file

At the time I have complete numbering of the connections at the schematic circuit and at the CAD data too, I can progress to make the input file for translating into the GenRad™ system. This file is called "Circuit Description" and has *.*CKT* extension.

This file contains the declaration of each part of the circuit. In practice it means that this file describes how the testing points are connected to each component and how its nominal value and the toleration of the value from the datasheet. This is split into two parts. In the first part are the declarations only for describing the parts like as how electronic part is it and between how pins I can measure it (*Code 1*).

Declaration of this part in *CKT* file starts by header ***%CIRCUIT;***.

```
%CIRCUIT;
/* ***** TEST CIRCUIT ***** */
R00A   R      N27, N28;
C02A   C      N28, N73;
D04A   CR     C=N38, A=N14;
T01A   QP     E=N27, B=N31, C=N30;
T04A   QN     E=N35, B=N32, C=N34;
I31A   TL432  1=N7, 2=N41, 3=N11;
...
```

Code 1 Illustration code of the first part of CKT

The second part of the *CKT* file corresponds to the named parts, its value or specific numbers in the case of integrated circuits, memories, processors, Connectors, transistors and so on. The declarations of passive components are included the tolerances if they are known (*Code 2*).

Declaration of this part of *CKT* file has the header ***%VALUE;***.

```
%VALUE;
/* ***** VALUES ***** */
R06A   =      47.5K, 1%;
C02A   =      4.7U, +20%, -10%;
D22B   =      9.1, 2%;
I01A   =      NOTEST, MSG='Spezielle Test';
T31A   =      MSG='Spezielle Test';
...
```

Code 2 Illustration code of the second part of CKT

As you can see in the picture above (*Code 2*), especially cases if the component does not have any measurable value or if we have another specialized tester for any component, we can use the variable ***NOTEST*** or only display the message by command ***MSG='...';***.

At the end of naming and declaration there is the last third part. Here are naming used test points (nails) as the temporary pins (*Code 3*). These pins will be renamed in translation process and the temporary pins will be renamed onto the fixed one. But I will write about this hereinafter.

The declaration of header of the last part is ***%ADAPTOR: 2281 TEMP;***, where the word *TEMP* means temporary pins.

```
%ADAPTOR: 2281 TEMP;
/* ***** PINS DECLARATION ***** */
F1     =      N1;
F2     =      N2;
F3     =      N3;
F4     =      N4;
F5     =      N5;
F6     =      N6;
...
```

Code 3 Illustration code of the third part of CKT

3.1.4.1. List of possible shortcuts for declaration components

In the table hereinafter (*Tab. 2*) we can see possible shortcuts, which can be used for the automatic testing of components. For these components there is a program library for testing inside the main system. For the other components there must be the testing routine code programmed manually by using available the commands.

Jumper	***J***	Induction	**L**
Contact normally Open	***NO***	Diode	**CR**
Contact normally Closed	***NC***	NPN transistor	**QN**
Resistor	***R***	PNP transistor	**QP**
Potentiometer	***RV***	Zener diode	**VZ**
Capacitor unipolar	***C***	Thyristor	**SCR**
Capacitor bipolar	***CP***	N JFET	**NJFET**
Tantalic capacitor	***CP1***	P JFET	**PJFET**
Silicon-Controlled Rectifier	***SCR***	Fuse	**F**
External Connection	***EXT***	Open Jumper	**OJ**
Bank of Components	***BANK***	Digital Component (IC)	**IC, DIC, type**
Analog Component	***ICA, IC***	Cluster (a group of component)	**CLUSTER**

Tab. 2 Possible code shortcut for automatic control of components [3]

For these components there exist explicit libraries, which are included in GR228X software.

3.1.5. Debugging when translating *CKT* to *TPX* file

Once the *CKT* file is complete, we can translate it by using the 228X software, which is especially developed for our testing machine GenRad™ GR228X. In the process of translation the *CKT* file is checked for any errors. If there will be any mistakes found, the translating will break and write the error on display and into the *ERR* file. If

the translating is done successfully, the *TPX* (*TPG*) file is made at the output in the same directory as in our *CKT* file.

The errors and mistakes which can originate are mainly the missing semicolon, bad format of testing points, bad declaration of value of component or bad format of writing. These problems are marked into the *ERR* file, what is our *CKT* file with warning, error and other comments inside the main program text. In the comment we can clearly see where and what the problems are (*Code 4*).

```
   30 :%CIRCUIT;    /* ***** DECLARATION OF COMPONENTS ***** */
   ...
   254 :/* ***** DIODES ***** */
   255 :D01A CR     C=N2, A=N73;
   256 :D01B CR     C=N6, A=N103;
   ...
   408 :%VALUE;     /* ***** DECLARATION OF VALUES ***** */
   ...
   633 :/* ***** DIODES ***** */
   634 :D01S =      750M, 10%
###         ^
### ERROR NO.   1 AT LINE 634:
### CDL1- Device not previously defined.
###
   635 :D01B =      750M, 10%;
###         ^
### ERROR NO.   2 AT LINE 635:
### CDL1- You have a syntax error.
###
###         ^
### ERROR NO.   3 AT LINE 635:
### CDL1- Invalid value item.
###
###                          ^
### ERROR NO.   4 AT LINE 635:
### CDL1- Characteristic value must be given.
###
```

Code 4 Error message in ERR file

As we can see in the illustrated case above (*Code 4*), the error commands are written clearly with the signing to the place of error. In this case I explain the mistakes in two cases.

The first error was the different part name than it was declared in the part of declaration of measuring pins – line number 255. As we can see, the declared name of component is D01A, not D01S!

The second error is missing operator. In this case it is a semicolon at the end of the code at line number 634. Every code line must end by a semicolon!

The next errors are given by the missing operator at the previous command. The translator takes it as one line and that is why the errors are reported as “Invalid value item” and “Characteristic value must be given”. These errors we can skip, because at next translation after repairing the previous two errors will be repaired automatically and the program will be without errors.

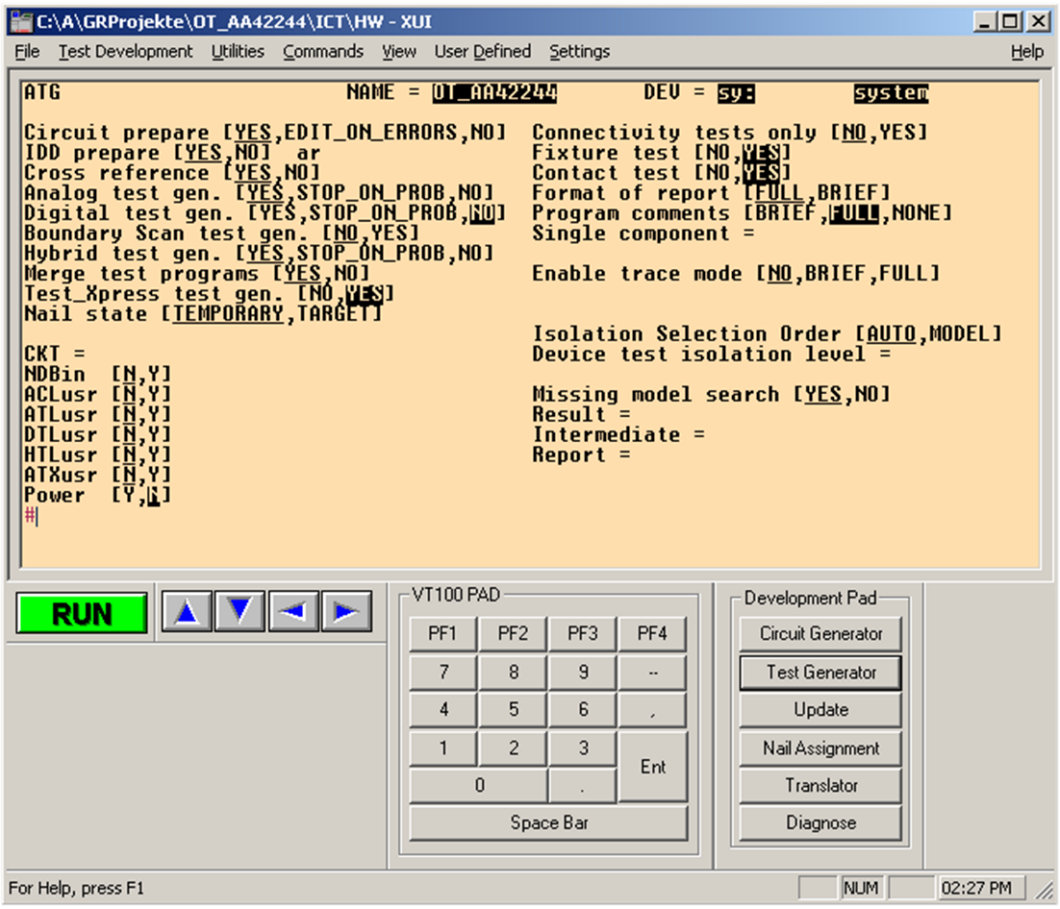

Fig. 16 Test Generator window of 228X program (CKT to TPX)

For translation of *CKT* files we will use the *ATG* (Automatic Test Generator) subprogram – the button called Test Generator (*Fig. 16*). As was describe over, this will make the *TPX* (*TPG*) file from our *CKT* file.

This *ATX* contains range of settings which are necessary for right translations of *CKT* file. I will explain shortly only the main for my project. The next are described in [3].

Circuit prepare:	• The setting of the possibility to make the *ERR* file with errors with automatically stop after pass (YES), break translation after found error with place to replacing it (EDIT_ON_ERRORS) or the WOR file is exist and the CKT file was changed (NO)
IDD prepare:	• This choice allows to create the *IDD* file. This file is necessary for testing the circuit automatically by UUT. This file contains the machine binary code.
Analog test gen.:	• Enable the analog test for analog components
Digital test gen.:	• Enable the digital test for digital components like as logic circuits
Nail state:	• Determine, if the selected pins are temporary or permanent (at this depend the extension of output file – temporary has *TPX* and permanent *TPG*)
Program comments:	• Indicates, how explicit the comments will be added into the result file of test program • The brief comment only pages header, while the full comments everything and every loop

Tab. 3 Table of description of the ATG window

3.1.6. Process of changing of pins from temporary to permanent

In the process of renaming the pins from temporary to permanent resort the changing of numbers of pins by program algorithm. Every test step can used only 2

relay pins of a group of 8 of the relay multiplexer. That is a requirement of the hardware construction of the tester.

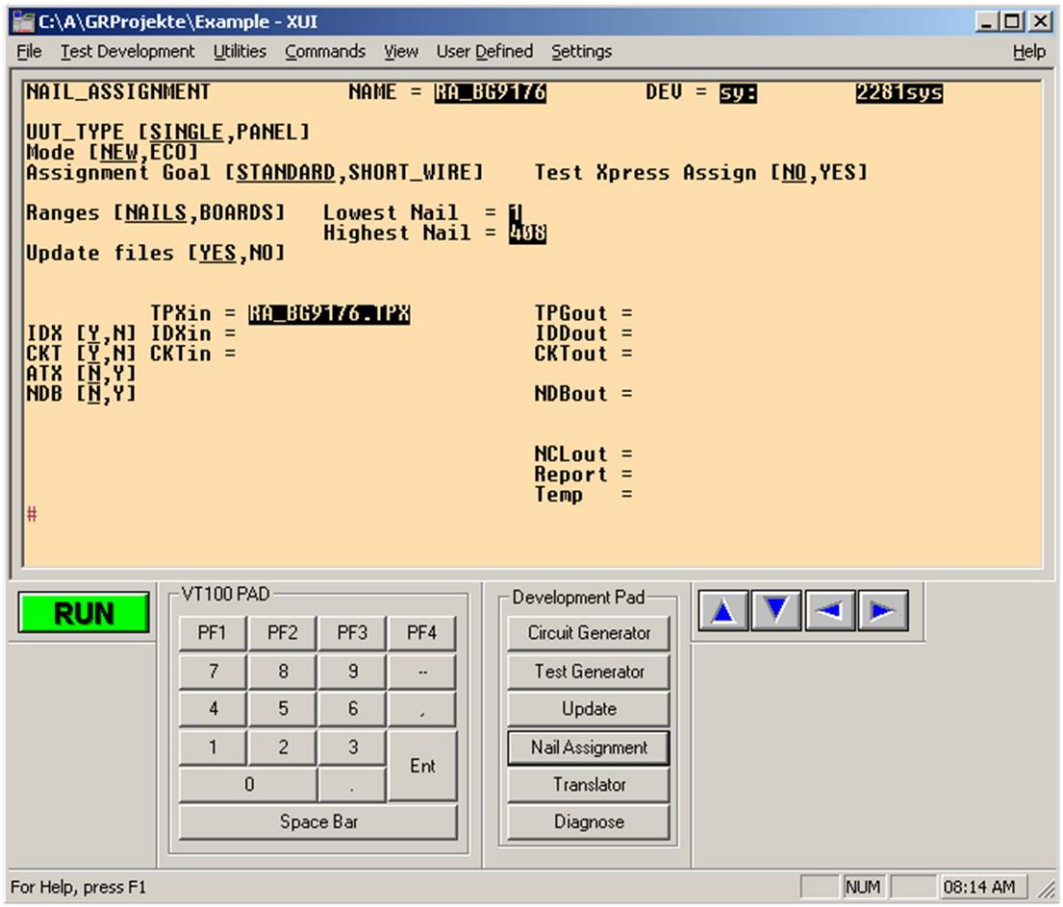

Fig. 17 Nail Assignment window of 228X program (Temp to Perm nails)

At the window of Nail Assignment we can see seven variable options. As at previous ATG window I will describe only the main choices. For more information you can use the GenRad™ manual [3].

UUT_TYPE:

- This setting describes what kind of PCB we are testing
  - For one single board choose SINGLE
  - For more PCBs or if measured PCB is only part of bigger unit, select PANEL

Mode:	• This setting depends on the fact, if we have built tester yet or not. ○ If we are building the new tester, choose the choice NEW

Assignment Goal:	• Describe the Nail Renaming logistic
	  ○ For standard logistic with the most compact and efficient nail assignment choose STAND-ARD
	  ○ For what shortest wires between nails and UUT choose SHORT_WIRE

Test Xpress Assign:	• Controls whether the Probe Report tool is running
	  ○ For the no XPRES TEST chose NO
	  ○ For the XPRESS TEST chose YES

Ranges:	• Indicates the range for using nail numbers when renaming
	  ○ For the specification of nails set NAILS
	  ○ For the specification of nails on more boards set BOARD
	  ▪ Lowest Nail – lowest available nail
	  ▪ Highest Nail – highest available nail (limited by used tester)

Update Files:	• Enabled the updating of existing *TPX*, *IDX*, *CKT* and *ATX* files
	  ○ For update set YES
	  ○ For let the files without any changes set NO

Tab. 4 Table of description of the NAIL_ASSIGNMENT window

```
/*
TEMP NAIL NUMBER -> ASSIGNED NAIL NUMBER
-----------------------------------------------------
*/

%NAILMAP 2281 NEW;

F1->  F141 ;
F2->  F123 ;
F3->   F65 ;
F4->   F93 ;
F5->  F142 ;
F6->   F34 ;
F7->  F104 ;
F8->   F19 ;
F9->   F20 ;
F10->   F40 ;
F11->    F2 ;
F12->  F105 ;
...
```

Code 5 Illustration code of NDB file of renaming nails

The next function of Nail Assignment function is to make the *TPG* file, which is similar as the *TPX* one, but it works with permanent nail numbers instead of the *TPX*, which works with temporary numbers. At the same time with creating TPG file, there are IDD, CKT, NBD and NCL files created. What contains CKT file, I described above (*Chap. 3.1.4*) and the next files I describe in one of following part (*Chap.3.1.9*). Here I must only state the output *CKT* file contains the permanent nails with table of re-named nails at the end of *CKT* file like is at the picture above (*Code 5*).

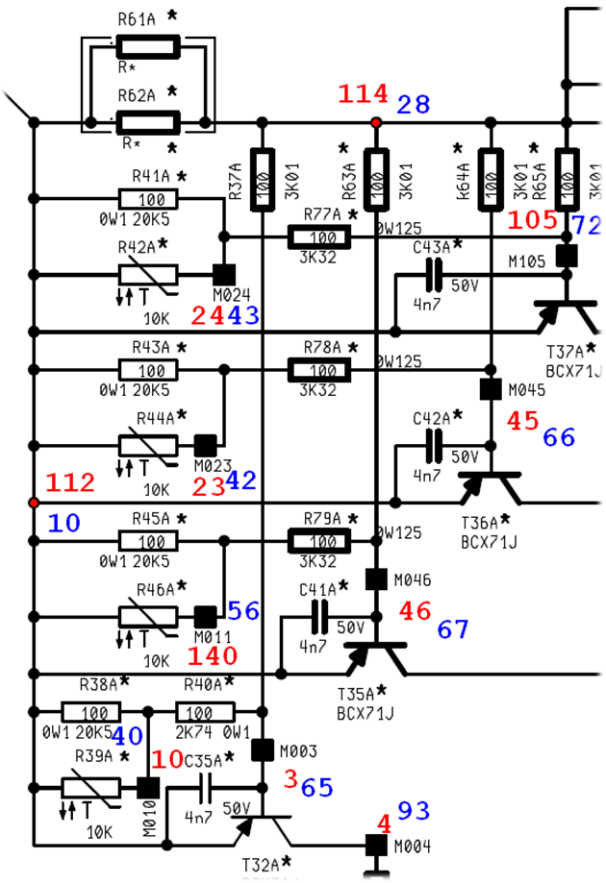

Fig. 18 Renaming the Temp (red) pins to Perm (blue)

3.1.7. Translation of *TPG* to *Machine Code (OBC)*

Once when we have translated the *CKT* and the *TPX* files to the *TPG* file correctly and all errors from the *ERR* file are repaired and changed to the temporary names of pins to permanent, which is in the *NDB* file, we can continue in translating the *TPG* file to *OBC* file. Now we will be working with new permanent pin numbers.

In this case the program is controlled to branching around any component or other errors as bad or missing automatic programs for control or syntax error. If there are any, the errors list will be in the *LIS* file. This file (*TPG*) is the final program code before final translating to machine code and we can write our own program parts for components which are not automatic program here. This concern of processors, memories, special circuits and components or for block part of components, which we are not able to measure directly with each other (e.g. parallel or serial combination of more components).

In my case I must add the dummy test for the integrated circuit I01A and I01B, which cannot be measured for functionality (*Code 6*). This means to test every pin except the ground against the VCC pin. In this case the VCC pin the Channel A with number of net 26 and the ground, what means reference point, is with number 4. Every pin should be connected to the VCC pin by protecting Zener diode and this test measure only inside connection between each pin and VCC one.

```
/* DUMMY TEST OF INTEGRATED CIRCUIT IO1A */

IO1A_2: SET SCAN AT (CHA=26:CHB=112:CHC=4:CHD=0);
        CLEAR SCAN;
IO1A_3: SET SCAN AT (CHA=26:CHB=71:CHC=4:CHD=0);
        CLEAR SCAN;
IO1A_4: SET SCAN AT (CHA=26:CHB=70:CHC=4:CHD=0);
        CLEAR SCAN;
IO1A_6: SET SCAN AT (CHA=26:CHB=124:CHC=4:CHD=0);
        CLEAR SCAN;
IO1A_8: SET SCAN AT (CHA=26:CHB=11:CHC=4:CHD=0);
        CLEAR SCAN;
```

Code 6 Dummy test for integrated circuit

As we can see hereinafter at the picture of 228X window (*Fig. 19*), here are not a lot of settings. We can choose only the Type of Listing, Disable General Warnings and set for how type of machine the program has been written. In this case we use the ICA subsystem, which is in BuS Elektronik.

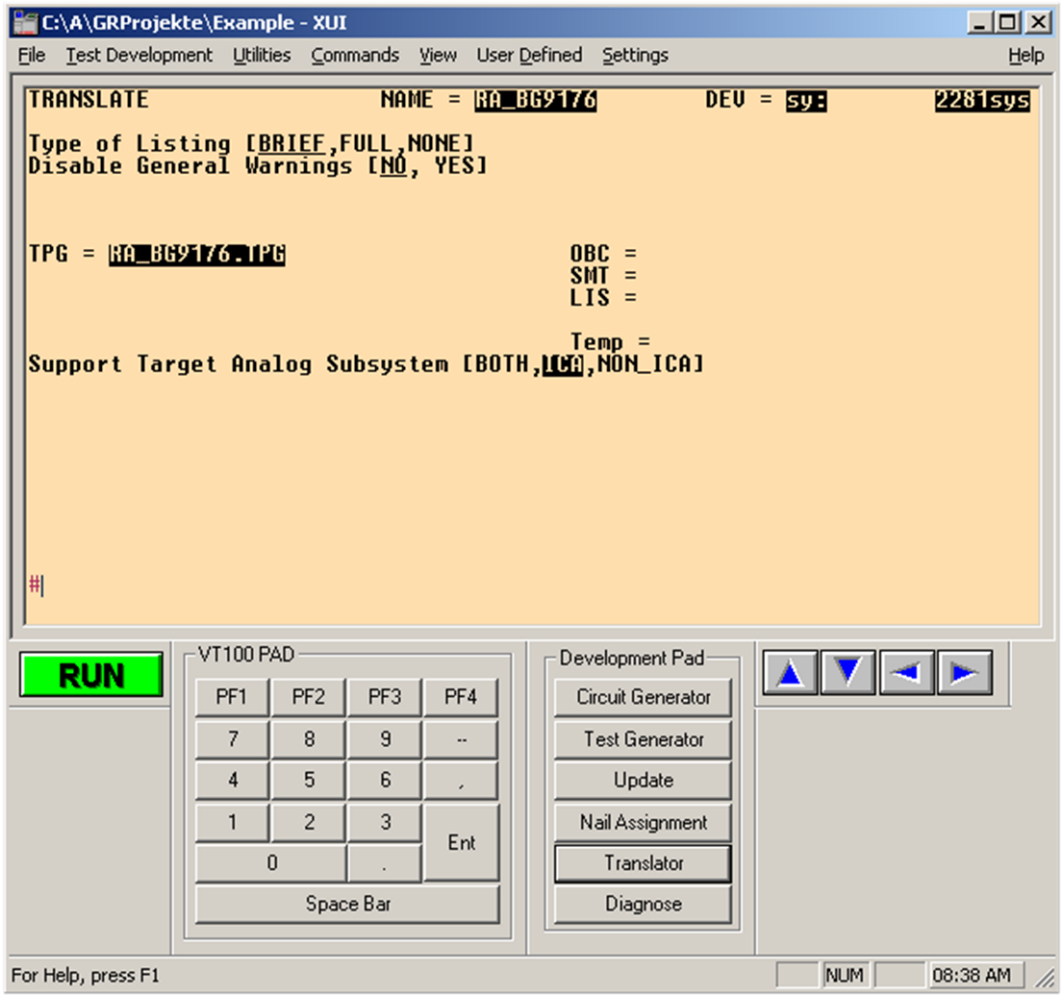

Fig. 19 Translating window of 228X program (TPG to Machine Code)

In the same time when the *OBC* file had been created the error and warning file *LIS* accrues too. The content of example is similar as the *TPG* file, but here errors are described in comments again like as in *ERR* file.

In the example of an error, we can see hereinafter (*Code 7*), where the translator found the branching error around the component with name R31A. That means this component cannot be measured, because another circuit is probably bridged with this resistor (*Fig. 20*).

```
/*
** THIS FORMATTED TEST IS NOT GUARDED. ADD GUARD POINTS AS
** NECESSARY TO THE "MEAS" STATEMENT (CHC=0:CHD=0).
*/

/* THE BRANCH STATEMENT MUST BE REMOVED TO EXECUTE THIS TEST. */


      USE FSUB=FAILSUB;  /* NEEDED FOR FIRST FORMAT TEST ONLY */
R31A: BRANCH R31AZ;
  MEAS R AT(CHA=11:CHB=7:CHC=0:CHD=0)
  CMSG='R31A' DMSG='1M' LO=2.575 HI=2.627
  V=0.2  MAX=2.601;

BRANCH R31AW;

R31AZ:
WRITE 'FORM TEST R31A WAS BRANCHED AROUND!%NL%';
```

Code 7 Branching error in LIS file when translating TPG to Mach. Code

This branching can be removed by adding the guard point to the circuit, which bridges measured component. In this case the measurement has been done by three- or four-terminal-measurement, where one input, one output and one guard point are used. This method is described in manual for GR228X systems [3] or on hereinafter picture from this manual (*Fig. 21*).

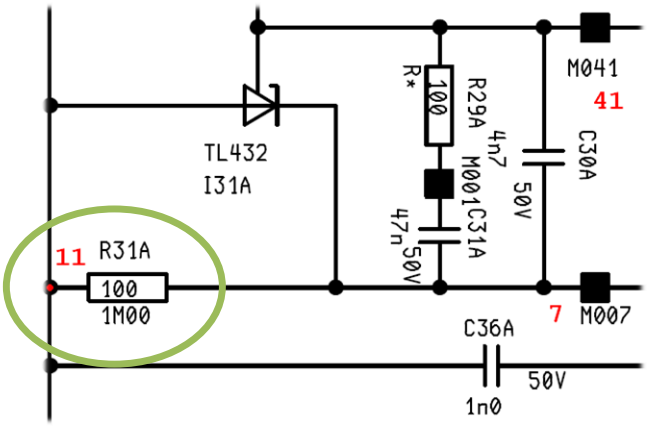

Fig. 20 Branched component (R31A)

In the real case it means that we need to ground the pin number 41. That causes the grounding the reference pin of controllable Zener diode TL432 (I31A). That switches off the transfer of cathode-anode and the measurement of resistor R31A will be possible.

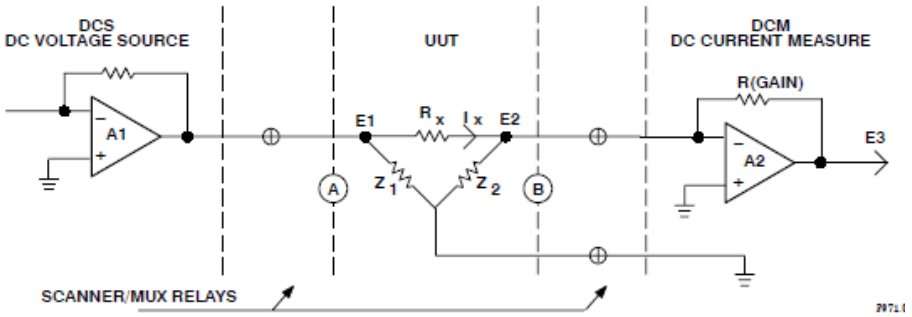

Figure 3-7 3-Terminal Resistance Measurement

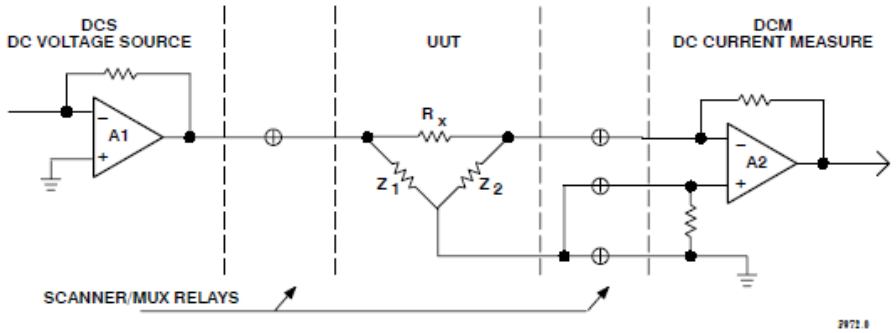

Figure 3-8 4-Terminal Resistance Measurement

Fig. 21 Guarded measurement by using 3 or 4 terminals

After the removing of the branch command the program looks like hereinafter at the figure (*Code 8*).

```
R31A:  /* BRANCHING REMOVED */
  MEAS R AT(CHA=11:CHB=7:CHC=41:GND=41)
  CMSG='R31A' DMSG='1M' LO=2.575 HI=2.627
  V=0.2  MAX=2.601;
```

Code 8 Removing of branching in the program code

3.1.8. Renaming of pins in CAD

Once we have done the Nail Assignment we should work with permanent numbers in CAD data. That is easier for us, because the final program for testing works actually with permanent numbering too. Because of this fact we have to rename the CAD design PCB from temporary to permanent. That we will do because these test points map will be given to the development department, where my fixture will be made.

The renaming from temporary to permanent have to be done in new layer because of clearance which pin is which before and after renaming. The new nets after renaming you can see hereinafter (*Fig. 22, Supp. IX*).

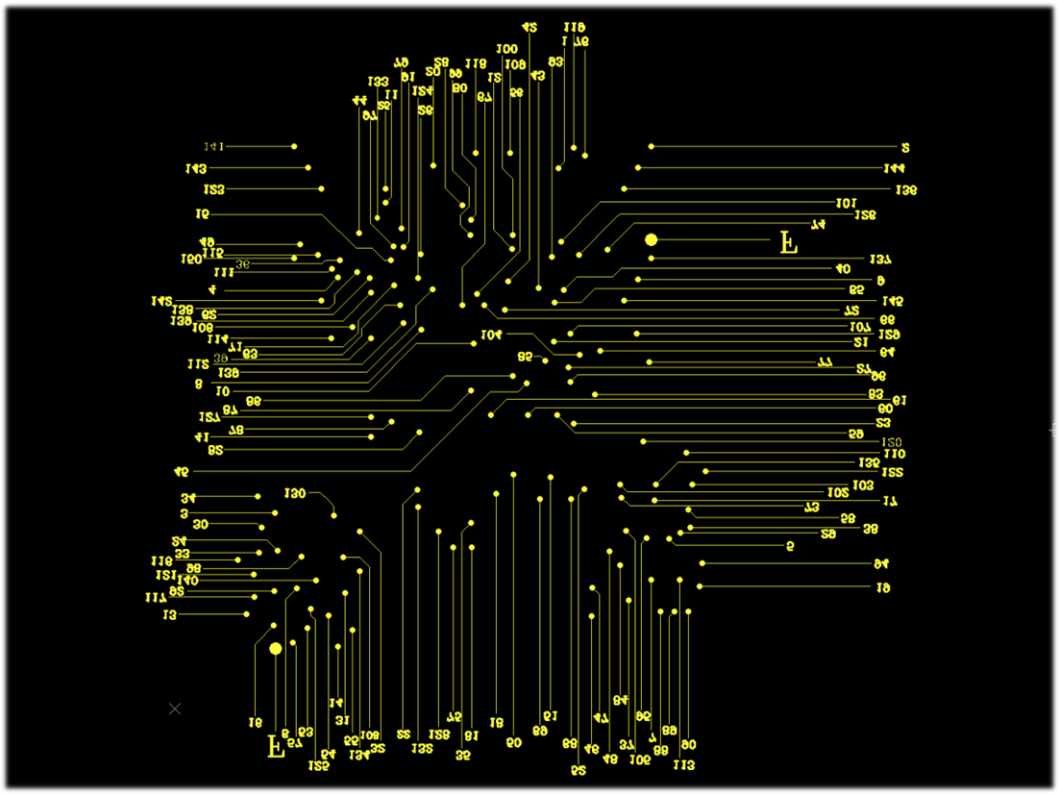

Fig. 22 Map of test points (with permanent numbering)

3.1.9. Description of files which had made automatically

The GR228X produces many files with every subprogram run. Here the files will be described, which had been created by whole process since translating the CKT file. The sorting of the files extensions will not be by the time when they create, but by al-

phabet. The files which will be described deeply above will be here described only casually with the reference to the appropriate reference.

ATP:
- Analog Test Program
  - Program AATG generates for testing analog components

AXR:
- Cross Reference Report
  - Report file that contains connection lists by components and by nodes and reports discrepancies

DBT:
- Debug Trace

ERP:
- Extraction Report
  - Report file that contains a summary of device node and nail entries in the *IDD* file

ERR:
- Circuit Description Error File (*Code 4*)
  - File containing CDL compile error messages

IDD:
- In-circuit Diagnostic Data File

IDX:
  - File that contains interconnect information used by the test generator and run—time diagnostics. It contains component pin data, node lists, and Driver/Sensor data
    - *IDX* = temporary nails

LIS:
- Error List File (*Code 7*)
  - Error messages include the statement at which the error was recognized

MLS:
- Merge Listing Report File
  - Report file containing result data for the merged test program that combines *ATP*, *DTP*, *HTP*, and *BTP*

NAR:
- Nail Assignment Report
  - Includes all the nail assignment information contained in the other reports, but is organized differently
  - It is sorted by assigned nail

NCL:
- Nail Contact List File
  - one-line description of each nail and its connection information

NDB:
- Nail Database File
  - File that shows mapping of temporary nails to actual nails, and selection of probe points and panel test options

NFR:
- Nail Fixture Report
  - Basic report that nail assignment produces
  - Includes all the nail assignment information contained in the other reports, but is organized differently
  - It is sorted by assigned nail.

NLS:
- Nail Assignment Listing
  - Provides information on the progress of the nail assignment function
  - Error messages and warnings that appear on the screen during the operation of nail assignment are written to this file

OBC:
- Object Code File
  - Binary machine data file

RPT:
- Analog ATG Report File
  - Report file that contains result data for all analog components tested, showing libraries used and problems generating tests

SMT:
- Symbol Table File
  - Binary machined data file
  - Contains pointers to labels and variables used when modifying or debugging a test set

TPG:	• Test Program (*Chap. 3.1.5*, *Chap. 3.1.6*)
TPX:	○ Source test program that includes the merged results of the *ATP*, *BTP*, *HTP*, and *DTP* files ▪ *TPX* = temporary nails
WOR:	• Circuit Description Work File ○ Circuit description file that has been compiled into a machine--usable format.

Tab. 5 Description of files with given extension [3]

3.1.10. Designing and making of fixture for tester

When we have completed the translating of programs and renamed the pins from temporary to permanent, we can proceed to design the fixture for tester. This we will do at the CAD software CAM350 too as a new layer. The outer dimensions are strictly given, but the placing on the fixture is at our decision. Because of the design of PCB was done as two boards in one panel and the length of fixture was sufficient I had designed the fixture for this big board where that an assembled sub-board can stay in the outer matrix.

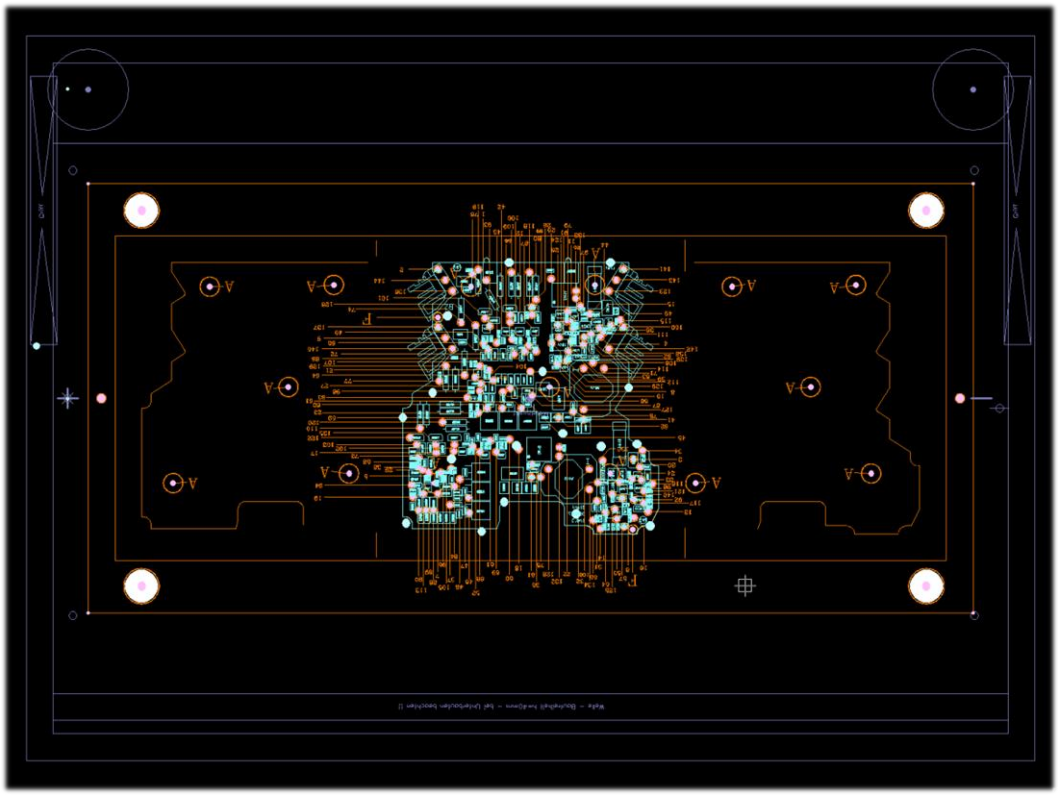

Fig. 23 Mechanical sketch of design of fixture with PCB

The fixture is made from two main boards, where the first larger board is used as a bearing, which will be plugged into the test machine. At this board two handles will be placed for easier manipulation and plug in/out from the body of tester. Next two homing pins will be here for the mechanical contact with the body of tester. Next here the hold parts of pins are mechanically connected which are wired to communication connectors which connect the pins to the inner multiplexer of the tester.

The second board is made as movable by spring connection. This board contains drill holes in which the test nails must have to go through and on which our assembled PCB will be laying. From this case the plastic pads must be here, which will buttress the PCB. The last mechanical components are the centering points (*Fig. 24*) which hold the PCB in the right position above the tips of nails. In the pictures above (*Fig. 15*, *Fig. 23*) marked by big letter *F*. In normal state this board is lifted and the nails are safe against damage.

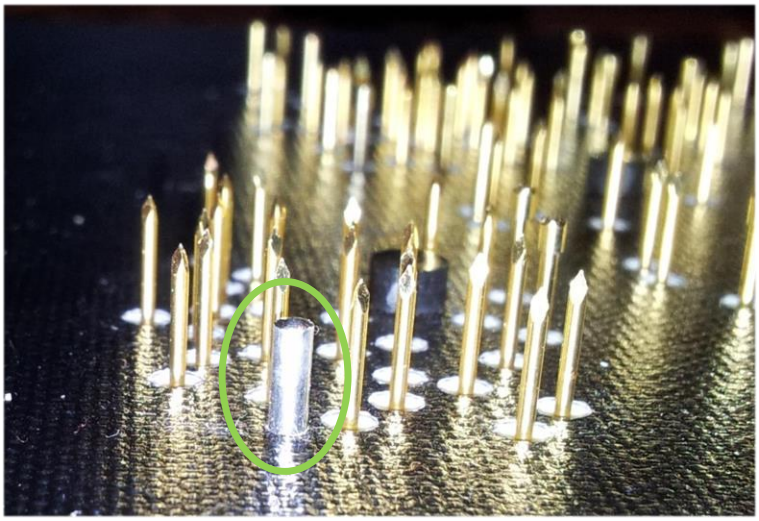

Fig. 24 Detail of the hold nail

When we take a look at the CAD picture above (*Fig. 23, Supp. XII*), we can see the main board drawing as the blue color and the movable smaller board as orange color. The placed PCB is drawn by azure color. Spring screws are in the corners of the smaller orange board and are colored by white circle with pink center. The last said component above are the buttressed pads. These are illustrated as the circle shape with pink center from what is brought out big letter *A*.

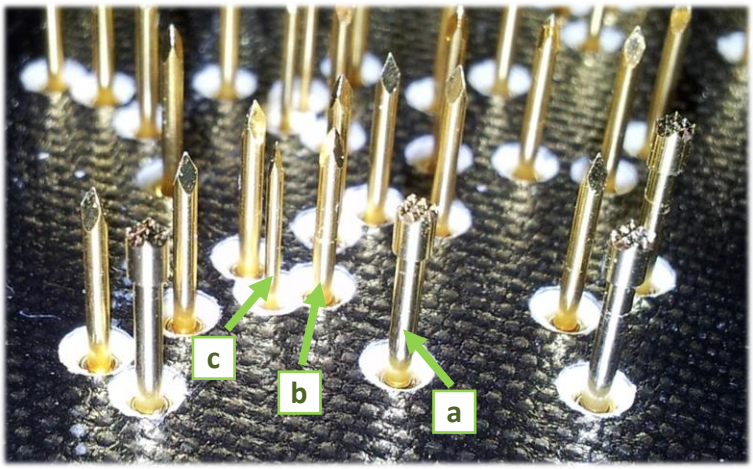

Fig. 25 Used shapes of the test nails

As I mentioned in the theoretical part (*Chap. 2.2.1.1*) we have many shapes of testing nails. In this case, three were three different types of nails (*Fig. 25*). The crown head (*a*), pyramid head about diameter of 1,7mm (*b*) and pyramid head with diameter

of 1,35mm (*c*). The crown head were used at bigger contacts like connectors or not SMD components. The pyramids were used for testing pads or vias. Here the pyramid shape is very useful because of the ease of removing the nail from the hole, because the testing areas are only the edges of the nail. Because of this, it cannot be hacked in the hole like as the cone shape, where is the contacting area the whole circumference. The diameter was given by the fact, how is the every nail far from the other. If the diameters here are bigger than 1,8mm, a larger one can be used, but for the places that have a higher density of nails the smaller ones can be used because of compliance with safety rules about minimal 1,8mm distance between each other nail (*Fig. 25*).

Once we have the design of the fixture complete we have to add it into the intercompany database of fixtures, where it gets itself company serial number by which it will be recognized in the tester automatically. Because of this fact, it must have the tester wired to itself with a serial number in binary format at the separate connector which is used only for this function. This adjustment needs special technical drawing (*Supp. XIII*), which will be given to the fixture development department, together with CAD design of our tester.

3.1.11. Testing of bugs in program and debugging

When the fixture was done from the development department I can debug my program directly on the test machine in real time with the sample of assembled PCB. For the test I used the tester GenRad™ GR2281 (*Chap. 2.3.1*) with permatech adaptor.

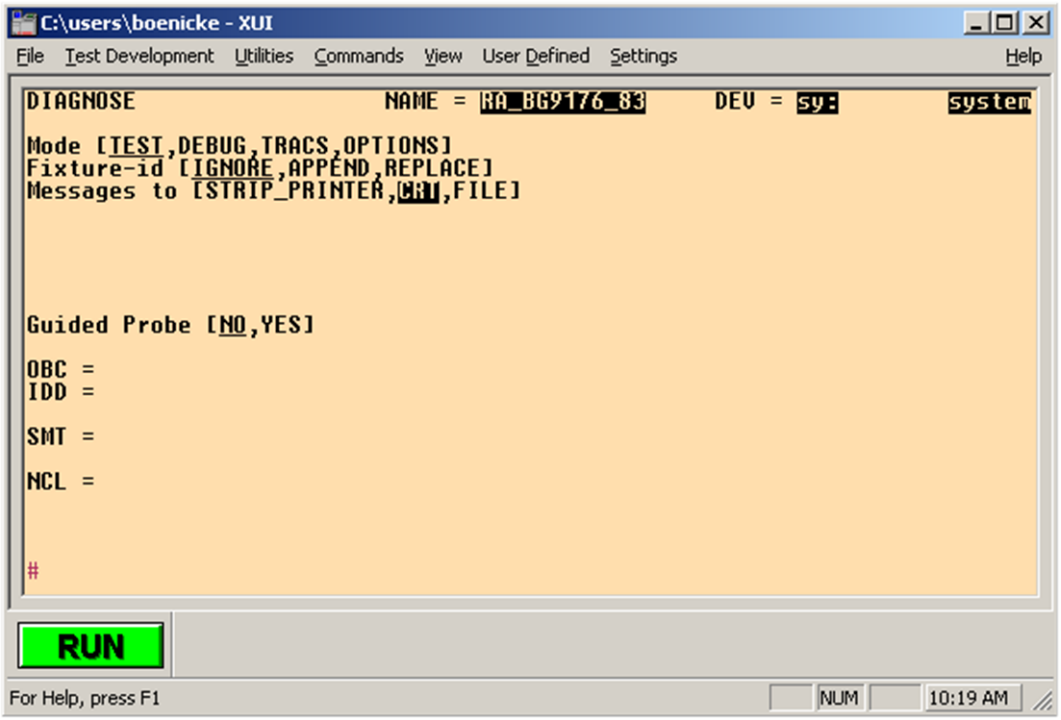

Fig. 26 Diagnose window of 228X program

This tester runs the same program 228X which I used for the previous steps and I used it for the debugging of my program. In this case, when the program runs directly on the tester, I can use the Diagnoses subprogram. This is aimed to automatic testing of PCBs in production. As we can see at the picture above (*Fig. 26*) the main window contains four settings. They are:

Mode:
- This setting describes how kind of testing we want use
  - For fully automatic test choose TEST
  - For debugging the program before sharp testing choose DEBUG
  - For automatic testing and also sending data to central system choose TRACS
  - For more settings of testing choose MODE

Fixture-id:
- This setting is for the right recognizing of tester and its program. The recognizing is given (binary) by wired fixture ID code on the connectors.

	○ If the tester does not have its fixture-id set IGNORE – but the name must be type into NAME ○ If the system converts the fixture-id to decimal value and then appends it to the NAME field, choose APPEND ○ If the system converts the fixture-id to decimal value and uses it for the NAME (it is not necessary to type the NAME manually), choose REPLACE
Messages to:	• Describes the place of write messages from testing ○ For printed result choose STRIP_PRINTER ○ For showing on monitor set CRT ○ For save result into the file set FILE
Guided probe:	• This option enable or disable the execution of the guided probe ○ For disabling of this function choose NO ○ For enabling choose YES

Tab. 6 Table of description of the DIAGNOSE window

After clicking on the run button the main tester window will start and we can see it hereinafter (*Fig. 27*). Now we will work directly with the test machine and the tester. After initializing the program we can see in the message part of the window, with which file we are working with, along with the date and time. In our case is it:

```
C:\users\boenicke\RA_BG9176_83.obc      24-MAY-13      10:21:30

TEST ]>
```

Code 9 Default state of message part of testing window

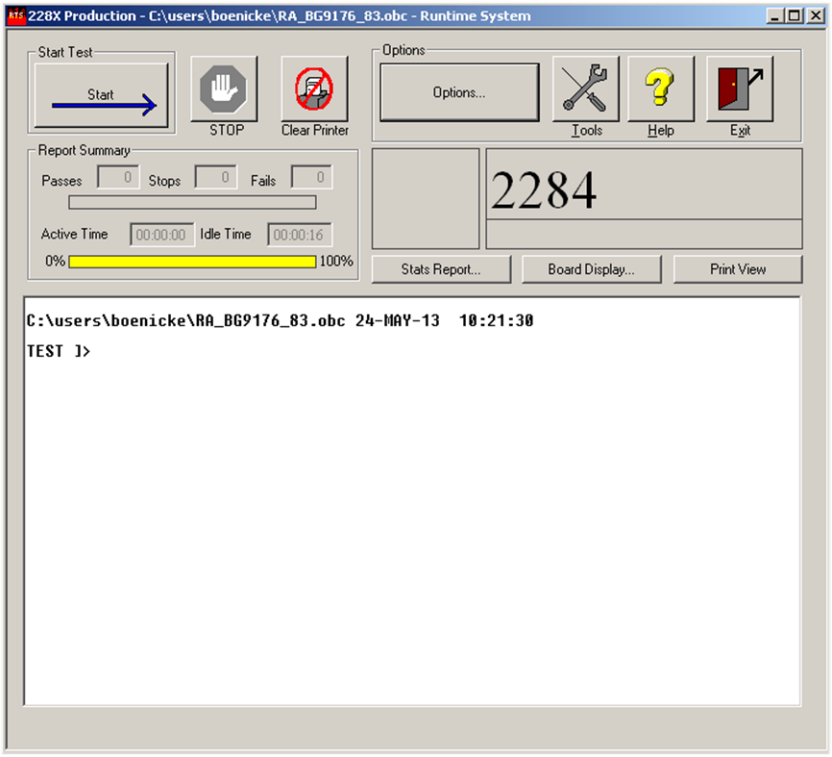

Fig. 27 Main window of 228X tester with default look

In this setting the testing program will working automatically and the result will be only pass or fail and the result in case of a failure. This mode is good when we have everything debugged with a well running program. But we need to debug the program, because we do not know, if is working well or not without any test run. Because of this we need to get to the debug mode, when we can run the program step by step with possibility to change the error for each component if will be any. To this mode we can get by writing the commands thereinafter (*Code 10*).

```
TEST ]> DEB <-

DEBUG ]> BEG=SETOHM /* SET THE BEGINING POINT */ <-
DEBUG ]> END=ADONE /* SET THE END POINT */ <-
DEBUG ]> DEB=FA /* RUN THE PROGRAM UNTIL FAIL */ <-
DEBUG ]>

DEBUG ]> DISP /* SWITCH BETWEEN TEMP. AND PERM. NAILS */ <-
DEBUG ]>
```

Code 10 Commands for get to the debug mode from the test mode

The first command changes the mode from the TEST to the DEBUG. The change we can see in a different marker. The next commands determine from what part to where the program works. In this case it is from the label SETOHM, which means the start position from the resistors test. The end of the loop will be at the command ADONE, which tells, that all components had been testing and the program is at the end. The penultimate command DEB=FA means, that the program will run automatically until the error happen. In this case it will stop running and show the error on screen with possibility to repair the error (*Fig. 28*). If the program passes after repairing, the program will run again and stop at the next error again. The last command is switching the nails numbers between temporary and permanent. This is useful for orientation in schematics.

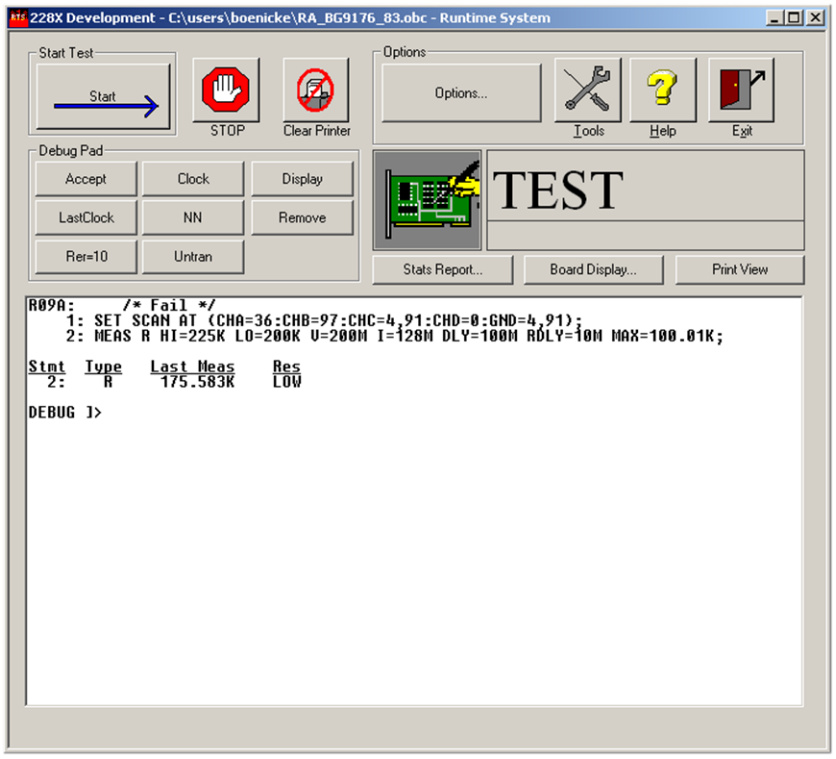

Fig. 28 Fail measurement message in developer mode

The failure message shown above, can be repaired in two ways. The first one is to correct the values or program part in corresponding *TPG* file and translate it and run program again (what have we done anyway) or repair the values directly in this window in running program. This is faster and easier than repairing, translating and run-

ning the *TPG* file after every error. But we must make a note what we changed, and after debugging, write the repair it into the *TPG* file.

Repairing of *TPG* file is easy and it was shown above (*Chap. 3.1.7*, *Code 8*). So here I show only how to repair the error in the running program by using the 228X Development window. Every line of code in the this window is numbered and is obvious because of the next steps. The error message is shown in format, where the label with the name of the component with a Passed or Failed status next to it. After this follow the lines of code with looks as in *TPG* file. After this we can see the number result from the test with the word explanation of the value (*Fig. 28*).

The repairing of error can look as in following example of code (*Code 11*).

```
DEBUG ]> 2 LO=170K <-
DEBUG ]> 2 HI=225K <-
DEBUG ]>



DEBUG ]> REM    /* RETURN THE CHANGES TO THE DAFAULT */
```

Code 11 Commands for repairing the wrong value range for passing

This code is wrote so, that the first is number of line, which we want to repair. In our case is it the second line, because 2. The next codes in syntax are what value we want to change and with what value. In our case it is low limit (LO) and we decrease the value to the 170kΩ. By the same way we can change the other values or change the values in other line. If we make something wrong, we can return the default values by writing the code REM (=remove).

If the repair is good, the component will be passed and we can continue in testing. The situation after good repairing we can see at the picture hereinafter (*Fig. 29*).

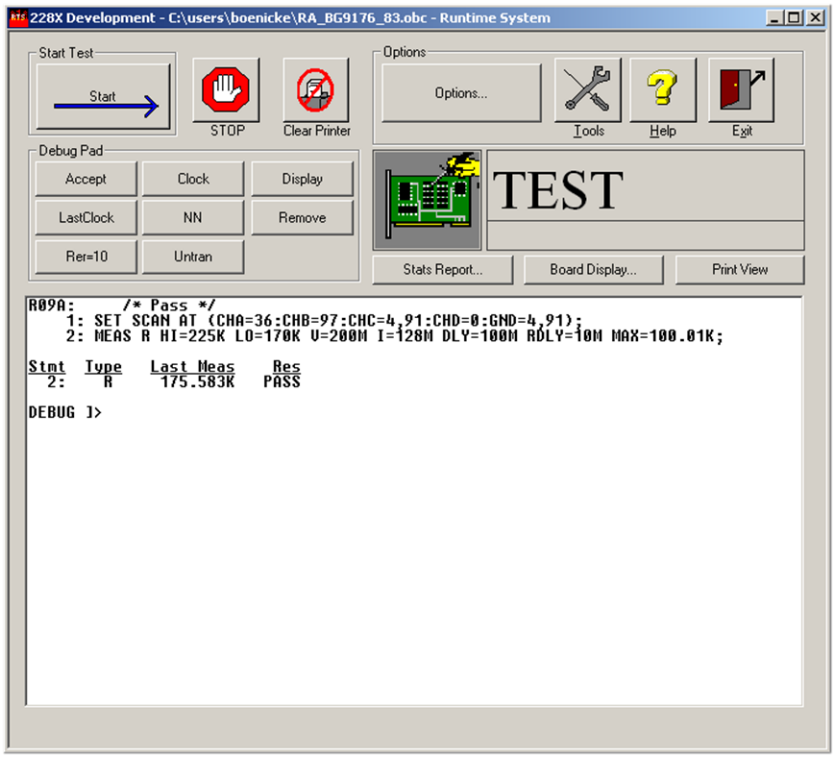

Fig. 29 Well repaired fail measurement

When the board tested well and passed it is necessary to mark it as passed. This is available and at the decision of the customer. In this case it was done by making the white dot at the bottom part of board as it shown at the thereinafter picture (*Fig. 30*, *Supp. XXXIV*).

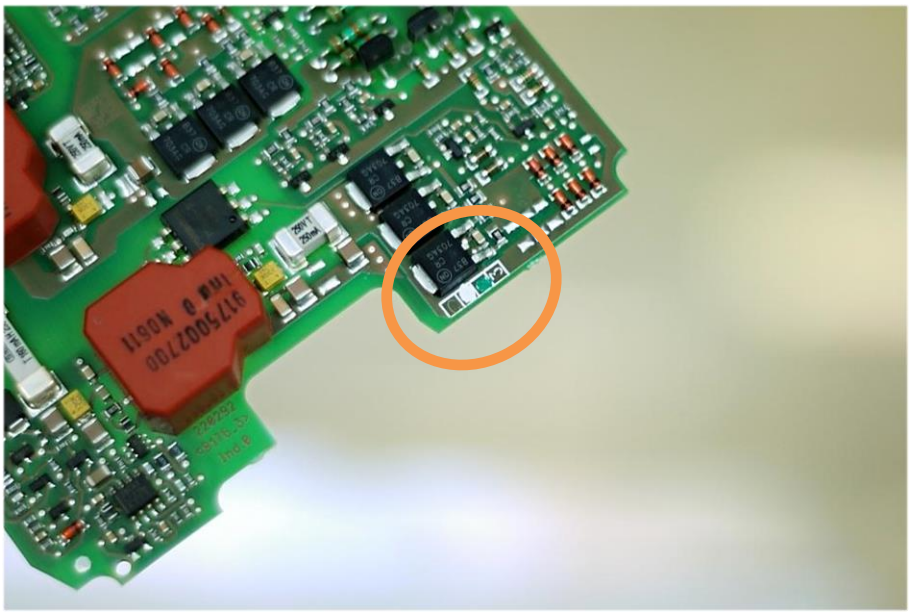

Fig. 30 Passed mark on the good board

3.1.12. Repairing of fixture

In the time of debugging of program I got the error, that the one pin is missing and that I cannot measure few components. The missing pin had number 32/15 (*Fig. 31*).

Because I had no time to repair the miss pin on the fixture before final testing, because the products must go to the customer. I had to remake the testing software to the temporary form where I had to bridge the missed pin and make the measurement from another nearest point through another component if it was possible.

From the picture hereinafter (*Fig. 31*) we can see, that the possibilities for measuring the components are followed. The resistor R05A we can measure in series with the resistor R06A or in series with R09A. That means pins 28/36 and 73/4 or 33/97, where the red number means the temporary pin and the blue one the permanent one. By these two possible methods we measured all three resistors. And the guarded point (explained above, *Fig. 21*) will be 33/97 for R05A and R06A in series and 73/4 and 34/79 for R05A and R09A in series.

Next we must measure the Zener diode D03A. This can be done from the pin 28/36 through resistor R05A or from 33/97 through resistor R09A. But in this case the measured value will be much smaller because of loses on resistor R05A or R09A.

The base probe for test of transistor must be connected into the pin 73/4 or 28/36 through any resistor. The last component, the capacitor C03A cannot be tested, because of the resistance of all resistors are too big for right measurement.

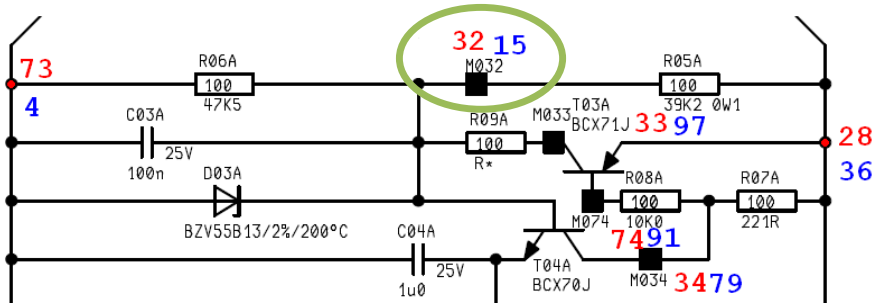

Fig. 31 Bridged of missing pin number 15

These changes were returned, after the fixture was repaired, at the default values and settings.

The steps of repairing the fixture itself are to make a new CAD layer with the right numbers and position of the new pin, remove the bad pin from fixture, drilling the new hole into the permatech adapter, place the reduction plate with new pin to the fixture and wired the pin to the right pin at the multiplex connector.

CAD designing of the reduction with new pin we can see hereinafter on the picture (*Fig. 32, Supp. XIV,* Supp. *XV*). In this case the diameters of the drilled holes will be different than at the normal adapter, because whole pins must go through. The new diameters of holes will be now in code D166 or 1,70mm instead of D139 or 1,02mm.

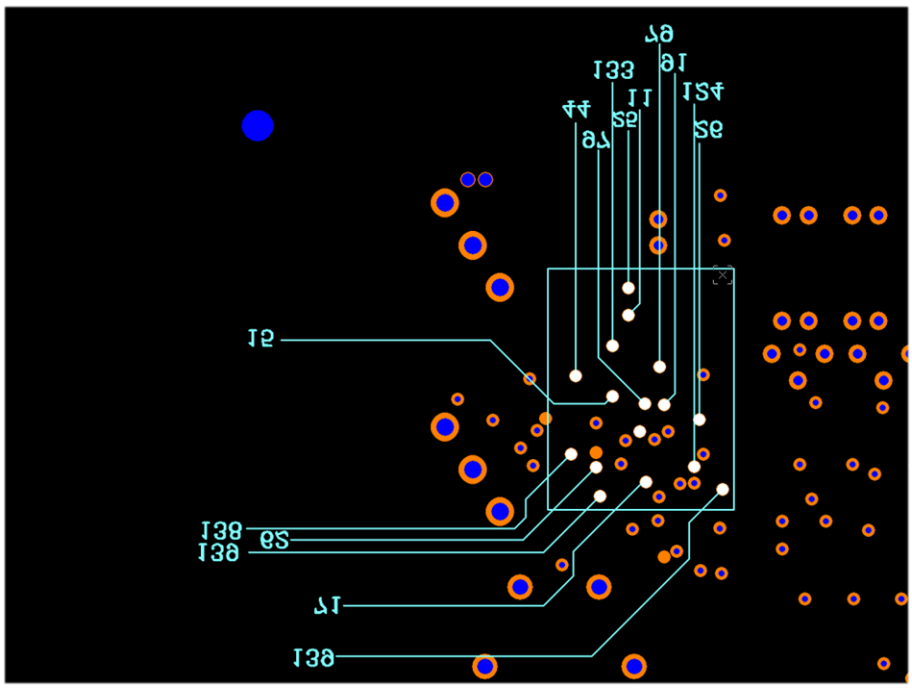

Fig. 32 CAD design of reduction pad with new pin

3.2. Calculation for request

This calculation will be for another order than the main theme of my diploma thesis and will be only for illustration purposes on how to make the preproduction calculation for the customer price request.

3.2.1. Description of calculation table

The calculation arch, as we can see it in the supplements (*Supp. XVI*, *Supp. XVII*, *Supp. XVIII* and *Supp. XIX*), the first page contains the header (*Fig. 33*), where the number of request, date of making calculation, name of the customer, the model number and the load of order.

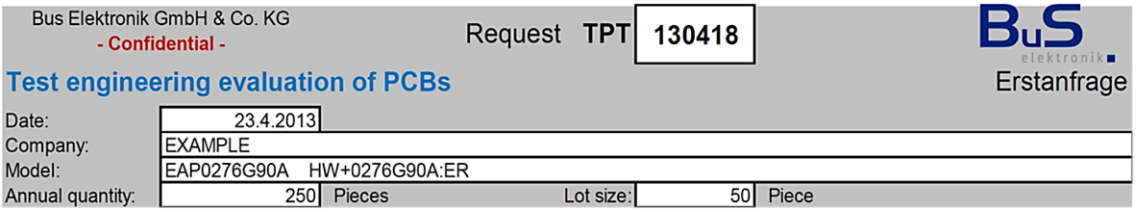

Fig. 33 Header of calculation

Under the header follows the calculation for each test procedure which can be done at the ordered board and the pre-test necessary operations, e.g. the programming of the processors before placement. Next are here the test methods as I wrote above.

The possible methods are:

- Flying Probe test
- ICT
- HV test
- Functionality test
- Functionality test 2
- Functionality test 3
- Run-in test with oven

Every method has its own sub-calculation (*Fig. 34*) for the works which are necessary for making the whole tests. What each cell means I will describe in the next chapter.

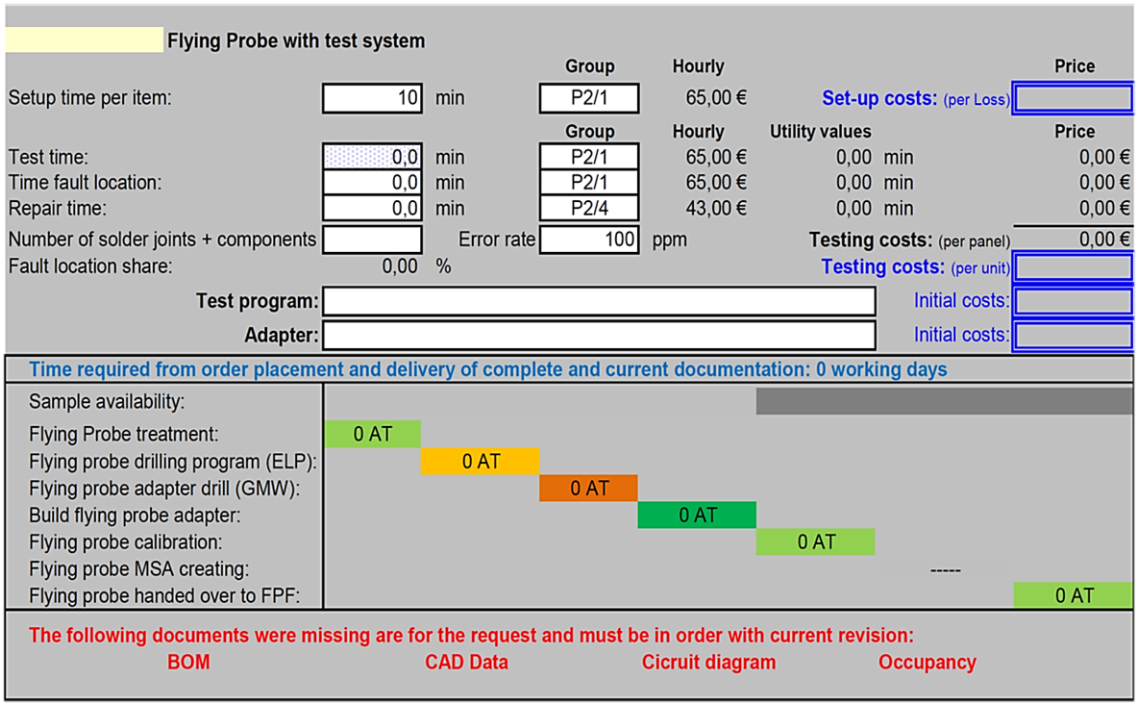

Fig. 34 Example of sub-calculation for one test procedure

And at the end of whole calculation (*Fig. 35*) are the places for other costs, scraping rate, total costs and remarks plus the editor name.

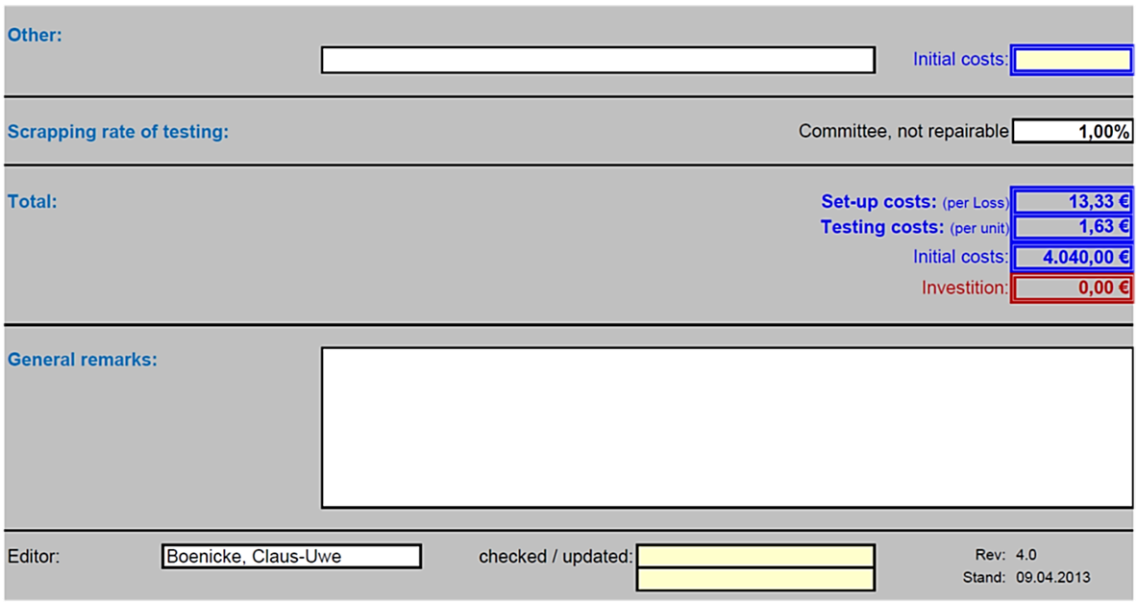

Fig. 35 The final part of whole calculation

3.2.2. Explanation of several calculations in calculation

Because in this request was only a request for the ICT test, I will describe only this part of the calculation. The following parts are similar in analogy with the ICT test.

3.2.2.1. Cost part of sub-calculation

In this part there will be the calculation of the preliminary price of testing of the order (*Fig. 36*). It is only a tentative price because we do not know how big the final cost will be, but the difference between this price and the final price should be the smallest.

ICT with Test system GR228X								
			Group	Hourly				Kosten
Setup time per item:	10	min	P2/2	50,00 €	Set-up costs: (per Loss)			8,33 €
			Group	Hourly	Utility values			Kosten
Test time in use:	0,94	min	P3/2	38,00 €	1,07	min		0,676 €
Time fault location:	2,00	min	P2/2	50,00 €	0,26	min		0,217 €
Repair time:	2,50	min	P2/4	43,00 €	0,33	min		0,233 €
Number of solder joints + components	600	Error rate	200	ppm	Testing costs: (per panel)			1,125 €
Fault location share:	12,00	%			Testing costs: (per unit)			1,125 €
Test program:					Initial costs:			2.290 €
Pematech adapter with 185 Nails:					Initial costs:			1.750 €

Fig. 36 Sub-calculation for ICT test (cost part)

Setup time per item

- says, for how long time will last the testing of one board in tester

Group

- means how requirements for the test machine intelligence are and how much educated must be the operator
- the first number in front of the slash means the level of the operator (P like as Prüfer = operator) and the number behind the slash means the level of the test machine (where is the number 1 the highest and 5 the lowest qualification)

- at dependence of this fact are given the prices of combination tester/operator per an hour (cell *Hourly*)

Set-up costs
- means, how much cost the test of one board per given time

Test time in use
- means, how long time will last testing of one board in tester with the operations like as input, output, mark the board as tested, etc.

Time fault location
- time necessary for find out the error on the board if there will be any

Repair time
- time needed for repairing the error on the board like as unsolder the wrong component, replacing it by new good one and soldered it

Number of solder joints + components
- tells how many solder joints and how many components are together on the board

Error rate
- probability how many error can cause in the whole number of connections/components from the previous paragraph

Fault location share
- error rate from previous two paragraphs expressed in percent

Test program
- contains the path to the file where test program is

Permatech adapter with N nails
- N is number of test nails necessary for well testing of whole board
- in this case it will be 185

The final price is provided by all used components, equipment, man power and the programming of software. These price calculations are calculated at the differ-

ent form (*Supp. XX*, *Supp. XXI* and *Supp. XXII*) where each used components or equipment separately noted with they own are prices and count.

3.2.2.2. Time part of sub-calculation

The time calculation tells the customer, when the order should be completed. The time of the production is in working days (AT means Arbeitstag = working day) (*Fig. 37*).

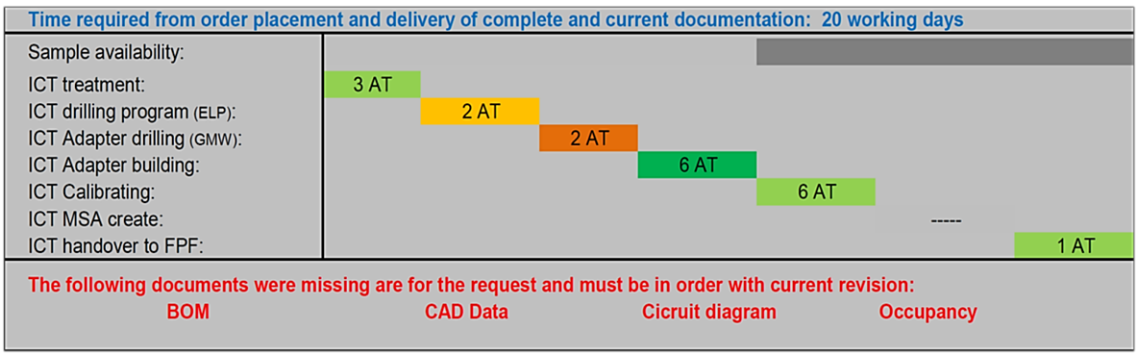

Fig. 37 Sub-calculation for ICT test (time part)

ICT treatment

- the necessary time for making and debugging the ICT program
- this part is calculated from the BOM (*Chap. 3.2.2.3.1*), where we multiplied the number of components by 25%

ICT drilling program (ELP)

- the time necessary for making of program for drilling is given by a flat rate and it is two days for adaptor with count of nails and pins under the 800. If is here more than 800 drilled holes, the preparing of program will last three days

ICT Adapter drilling (GMW)

- this time is given by flat rate too and it is two days

ICT Adapter building
- the time necessary for building complete adaptor including special additions and wirings
- for calculation are used the calculated times from adaptor modification part (*Chap. 3.2.2.3.4*)

ICT Calibrating
- the time necessary to calibrate and testing the fixture after building
- this part is calculated from the BOM (*Chap. 3.2.2.3.1*), where we multiplied the number of components by 75%

ICT MSA create
- time necessary for specialized MSA (Measurement System Analysis) test for automotive industry

ICT handover to FPF
- the time necessary for handover the tester to the production
- final time is given by sum of times from after tester done‘s part (*Chap. 3.2.2.3.2*)

In total time the development of the fixture, programming and the testing of each series last 20 working days. This time is counted for the whole order, but the default counts are for one piece from the whole order. Only the part like as fixture made or programming are for the whole order, because it is not necessary to make the new program and fixture for each board from series. The each part used for the calculation of each step is described in the next chapter.

3.2.2.3. Hidden part of calculation

In this hidden part of the calculation are details itemized and the sub-calculation of cost and time (*Supp. XX*, *Supp. XXI* and *Supp. XXII*). Here are the calculations for each component and for used material at fixture. From these calculations are following the time calculation in dependence of stock and the difficulty of montage.

3.2.2.3.1. BOM part

In the first part of the hidden part of the calculation (*Fig. 38*, *Supp. XX*) are itemized the used components for assembling the PCB like as e.g. resistors, capacitors, coils, active and discrete components, memories, processors and so on. Next is noted the price for the basic and expansion number of test points. From this parameter is depended the final test time for testing each board. At the last point is calculated the price of development of the ICT test program and its modifications. The unit of the programming is an hour. The other units are in pieces.

The E-Price means the basic price per unit (piece, hour). The G-Price means the final price for all components (E-Price multiplied by Stock).

For this part is done the particular calculation of necessary time to make a test and assemble the board. This is unfolding from the number of the pins and type of component. The necessary time to produce and test can be correct by the engineer's experience, but the default time is calculated automatically.

Stock	Description	E-Price [EUR]	G-Price [EUR]
0	Base price for 150 test points	xxx,xx	
0	Charge for each additional 50 test points	xxx,xx	
0	Measurement points (number of test points)	xxx,xx	
0	Resistors	xxx,xx	
0	Capacitors, Coils	xxx,xx	
0	Diodes	xxx,xx	
0	Z-Diodes, Voltage limiters, LEDs	xxx,xx	
0	Transistors (Bipolar)	xxx,xx	
0	FET´s	xxx,xx	
0	Quartz	xxx,xx	
0	Connectors	xxx,xx	
0	Combinatorial and sequence circuits	xxx,xx	
0	Bus driver and buffer circuits with tri-state outputs	xxx,xx	
0	RAM, EEPROM	xxx,xx	
0	DAC, ADC, PAL	xxx,xx	
0	ROM, EPROM,	xxx,xx	
0	Processors and their periphery	xxx,xx	
0	Operational amplifiers (per amplifier)	xxx,xx	
0	Optocouplers per channel	xxx,xx	
0	Relays	xxx,xx	
0	Power-MOSFET Controller (per output)	xxx,xx	
0	Power-Supply (each output voltage)	xxx,xx	
0	Sensors	xxx,xx	
0	Other	xxx,xx	
0	OpensXpress	xxx,xx	
0	Opens-Dummy´s (Dummy-Burst Disable-Section)	xxx,xx	
0	Frequency/voltage measurement	xxx,xx	
0	Boundary-Scan	xxx,xx	
0 h	Modification of the standard Rohprogrammes (ATO-Integration, Kontaktierungstest, German texts, sequence displays, Entladeroutinen Elko´s, Nutzensteuerung, version control) [in h]	xxx,xx	
0 h	additional manual work in data entry (no CAD data) [in h]	xxx,xx	
	Price of test program:		**0,00**

Fig. 38 Calculation of price of assembling PCB + test program development

3.2.2.3.2. Time Bill of works after tester done

The second part (*Fig. 39*, *Supp. XX*) is aimed at the calculation of the steps which are followed after the tester is done. Included here are the small batch testing for the testing of the small boards, next is the specifically MSA testing of boards which is required in automotive industry. The last two steps are the writing documentation as instructions for workers, making certificates, etc. and the handover to the production, which means the debugging of the prototype and making the final working version of the program and loading it into the tester in the production and familiarizing the worker with the program and the order.

Default time which is necessary for doing this part of sub-calculation is given by simply sum of the times in this part.

0 h	Small batch testing [in h]	0,00	0,00
0 h	MSA [in h] *at Automotive OBLIGATION*		
0 h	Creation of documents (test instructions, test certificate, ...) [in h]	0,00	0,00
0 h	Handover to the production [in h]		
	Total price of test program:		**0**

Fig. 39 Calculation of the works after done the test program

3.2.2.3.3. Calculation of ICT adaptor

Third part (*Fig. 40*, *Supp. XXI*) is aimed at the calculation of the fixture and its modifications which are necessary for making the working ICT and functionality test. The modifications can be the extended processors, memories, relays and the other circuits.

Calculation of ICT-Adapter

(adapter without creating documents, used number is entered)

Stock	Description	E-Price [EUR]	G-Price [EUR]
0	*Total number of test points*		
0	Base price project (up to 300 test points)	xxx,xx	
0	Surcharge for each additional 100 test points	xxx,xx	
0	CNC Set-up	xxx,xx	
0	Shorting plate	xxx,xx	
0	Ground plane	xxx,xx	
0	Two-sided contacting *(specifically calculated)*	xxx,xx	
0	*Number of test points on the second side*		
0	Additional circuits *(specifically calculated)*	xxx,xx	
0	2A small simple relay (incl. wiring)	xxx,xx	
0	2A small twin relay (incl. wiring)	xxx,xx	
0	8/16A large simple relay (incl. wiring)	xxx,xx	
0	8/16A large twin relay (incl. wiring)	xxx,xx	
0	Programmer for Processor	xxx,xx	
0	other	xxx,xx	
0	other	xxx,xx	
0	other	xxx,xx	
0	other	xxx,xx	
0	Hold-down pins	xxx,xx	
0	Standard wire (AWG 30)	xxx,xx	
0	Power wire (AWG26)	xxx,xx	
0	Additional charge for Twisted Pair, solder, coax connection	xxx,xx	
0	Spring contact with shell grid 100mil (2.54mm)	xxx,xx	
0	Spring contact with shell grid 75mil (1,90mm)	xxx,xx	
0	Spring contact with shell grid 50mil (1,27mm) *with wire*	xxx,xx	
0	Long stroke spring contact with shell grid 100mil (2,54mm)	xxx,xx	
0	Long stroke spring contact with shell grid (1,90mm)	xxx,xx	

Fig. 40 Basic calculation for adapter (particularly view)

In this part, the time which is needed for added circuitry is calculated separately. This is calculated from the part of added relays, where the calculation formula given by the form, if there is any added relay the time will increase about 8 hour.

3.2.2.3.4. Calculation of modification of adapter

Next part (*Fig. 41*, *Supp. XXII*) describes the calculation of the modification of adapters (fixture). In this case the permatech adaptor will be used. Here are included the price of bearings, pins, lifts and the moving plate on which will be lying the tested board (DUT).

	Pematech exchange use		
0	**Base price of adapter (315x210 without needles, including guide pins, top)**	xxx,xx	
0	Charge guide ball bearing 11mm	xxx,xx	
0	additional guide pin	xxx,xx	
0	additional support suspension 6mm	xxx,xx	
0	Snapper (LP bracket)	xxx,xx	
0	Eccentric	xxx,xx	
0	Lift	xxx,xx	
0	Needle guide plate (100x100 without needles, including guide pins)	xxx,xx	
0	Needle guide plate (150x100 without needles, including guide pins)	xxx,xx	
0	Needle guide plate (150x150 without needels, including guide pins)	xxx,xx	
0	Needle guide plate (200x150 without needles, including guide pins)	xxx,xx	
0	Needle guide plate (200x200 without needles, including guide pins)	xxx,xx	
0	Needle guide plate (250x200 without needles, including guide pins)	xxx,xx	
0	Double contacting *(specifically calculated)*	xxx,xx	

Fig. 41 Especially calculation for added part for permatech adaptor

Here the necessary time for building the adapter is calculated more complicated. The time calculation for this part is depends on the three factors which can change the final result. The first factor is the using of needle guide plate. If any are used, the time will increase about two hours. Second factor is the count of used tested nails. Here are two possible states. The first state is for the usage of less than 150 pins and the second state is for more than 150 pins. For the second case more time is added for the wiring, because it is less synoptic and more different to connect it well than in the lower density board. The third and last factor is adding an automatic lift. If we use it, the time will increase about eight hour.

This part of calculation is connected with the previous table with used components (*Fig. 40*).

3.2.2.3.5. Cost of ICT inspection time

The last part (*Fig. 42*) describes the lasting of the operations around the testing of board. This means inserting and taking out the board from the tester, creating a confirmation stamp about the testing and other completed tasks. Next I have described the final test run in the program and the sum of the pseudo-errors which can ensure during testing.

Cost of ICT inspection time

Stock	Description	Time unit [s]	Total [s]
0	Benefit		
0	Time for insertion of the BG / benefit of the adapter	1	
0	Time for taking out the BG / benefit of the adapter	1	
0	Time stamps (total time for all boards)	1	
0	Other work (Total time for all boards)	1	
0	Time programming (programming on one board)	1	
0	Test time (Program running time for a board)	1	
	Summe		***0,00***
3%	with pseudo-error component, other running costs		0,00
	Total time		**0,00**
	Testing time per BG		

Fig. 42 Time calculation of ICT test

The calculations in this part are simply multiplying the time unit by the stock. Only the pseudo-error time is calculated from Sum.

All values at illustrated pictures in this chapter (*Chap. 3.2.2.3*) had to be erased or replaced by x-values because of company secret politics for sensitive data.

4. Conclusion

In my diploma thesis I learnt how to test the electronic circuits and especially the printed circuit boards. Next I thoroughly explained the process from the beginning all way to testing the PCB from the phase of calculating the price request from the customer, through pre-processing the given data from customer, designing the fixture and programs and finally the testing of the series for customer before sold.

In the process of developing software for tester I had to debug the errors step by step until I got a good working result. Next I found the mistake while debugging the fixture. Here was the bad position of one needle and this position was doubled by another one. But because the customer was waiting for his order, it was the fastest and easiest way to remake the software for measuring without this point, which was possible in this case.

Because the customer had five modifications of his circuit, but at the same PCB I had to make five modifications of my program different for each board.

After finishing the order I could repair the fixture before it was saved in repository. This means removing the nail from the bad position and drilling the new hole for the new one, rewiring it and repairing all programs for measuring at the right position where it bridged over through this missing test point.

The next part of my diploma thesis was aimed at the calculation of the production at customer request. This was done for another order than the main theme and the idea of this part was illustrated on how to make a calculation or what the final calculation is exactly.

This was described in the two sub-chapters where the first one was the calculation of cost and the second part was the time calculation. Here I described all calculation and its sense.

This diploma thesis brings me the new sight into the problematic of production and testing the PCBs which I can use in the next professionally life.

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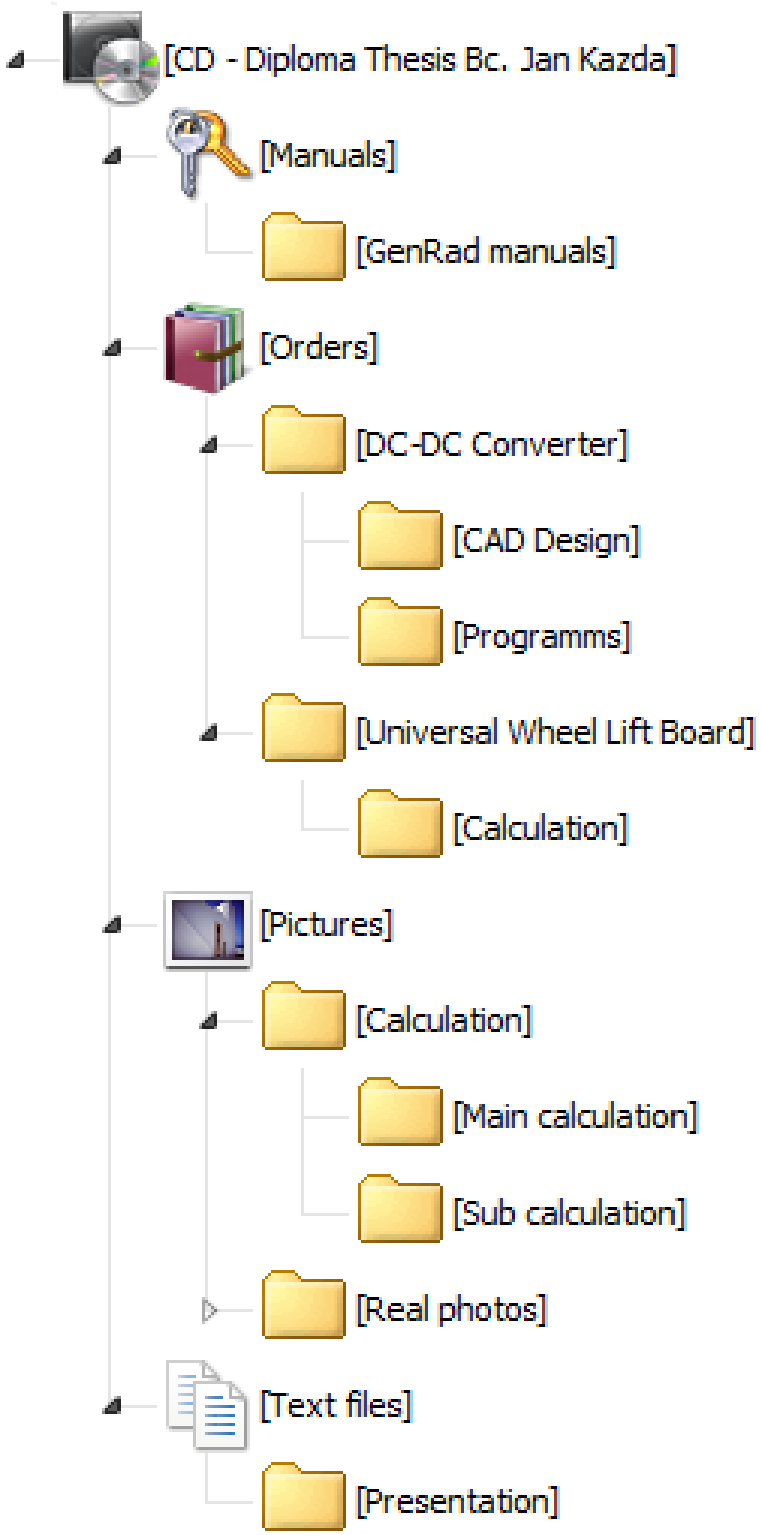
Content of pictures

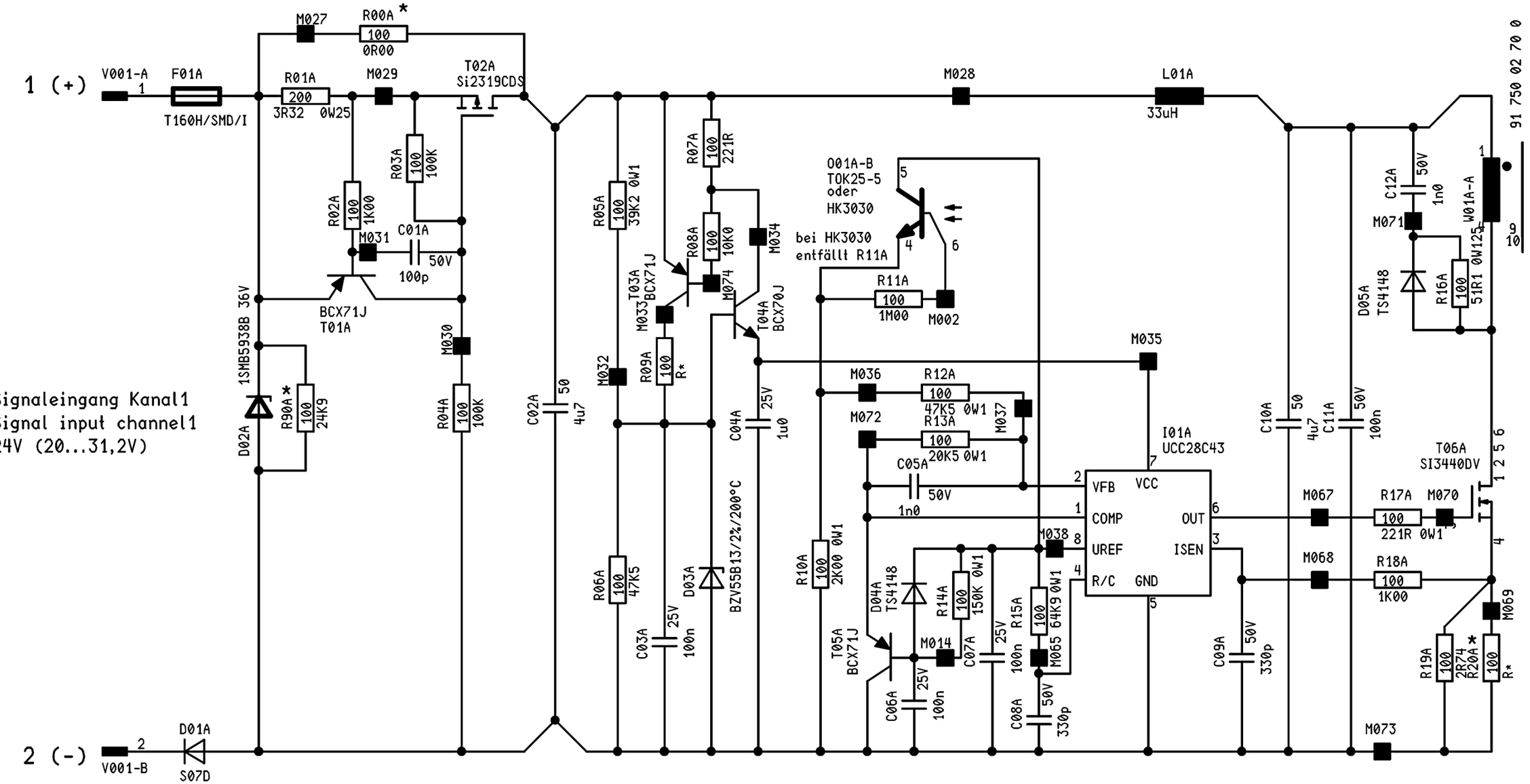
Content of tables

Content of codes

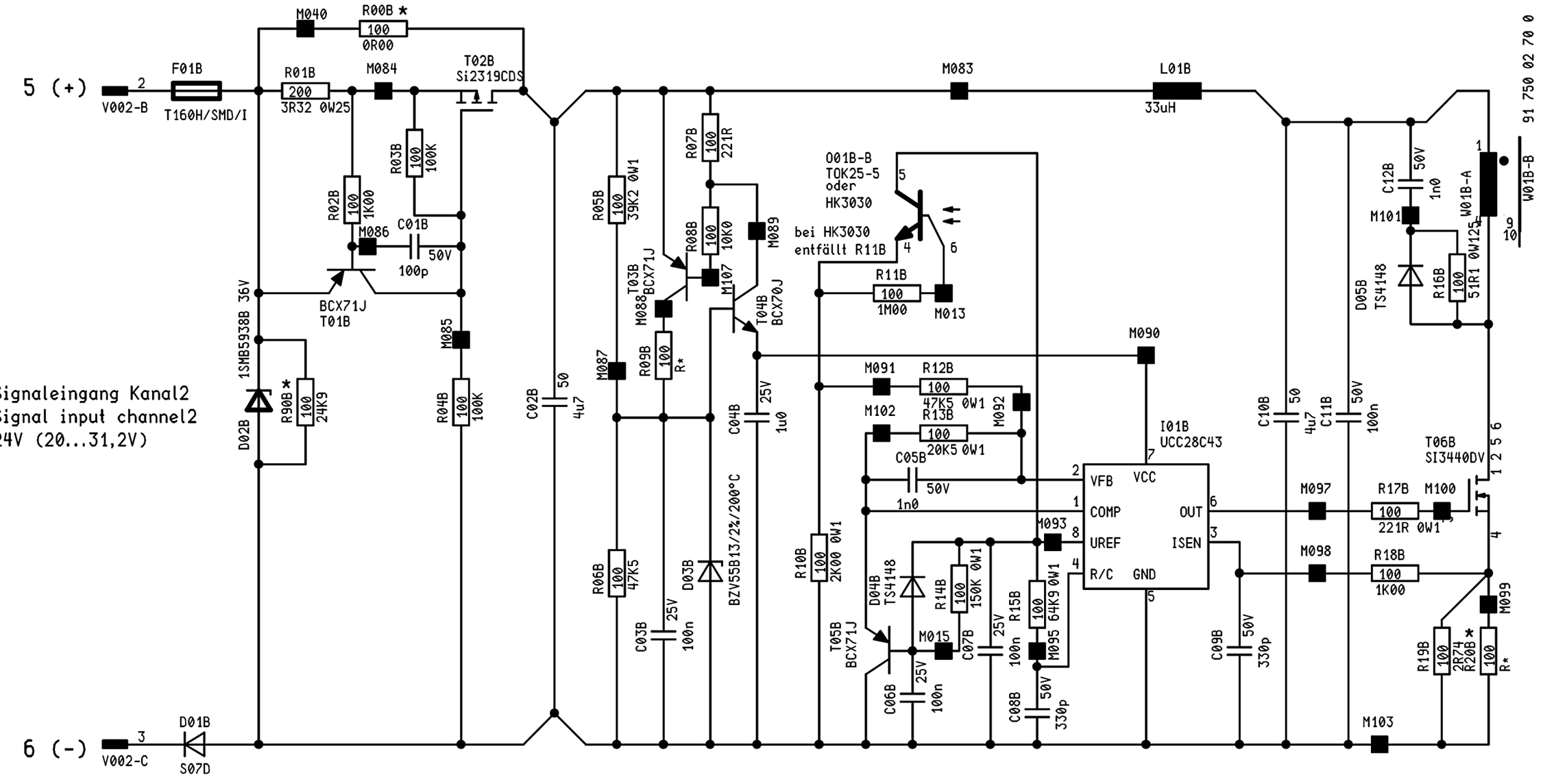
Content of enclosed CD



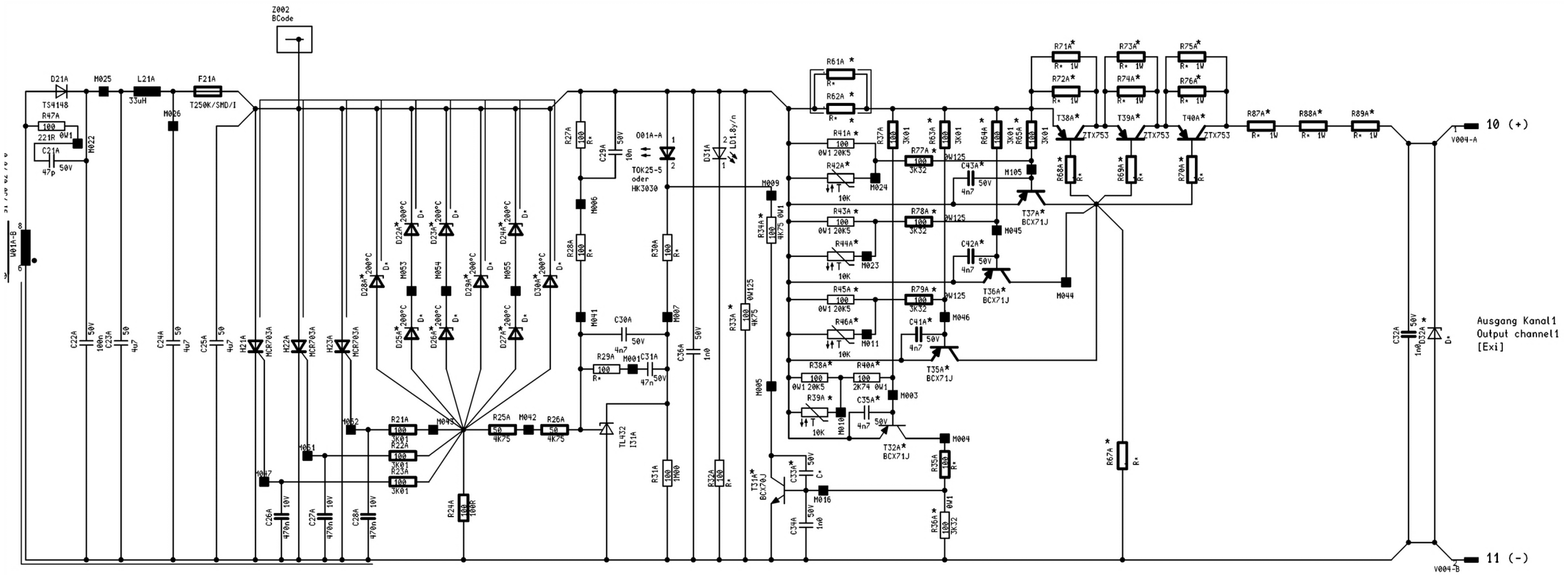
Content of supplements



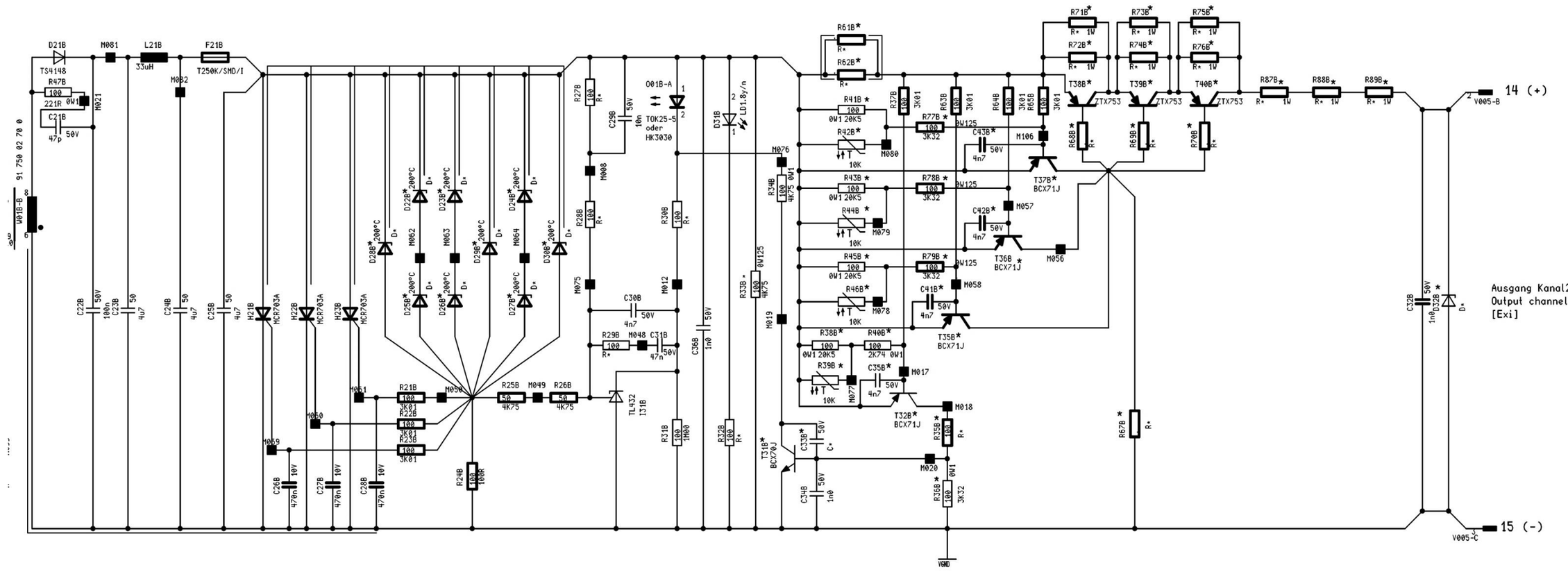
Supp. I 1ST part of schematic circuit – Channel 1



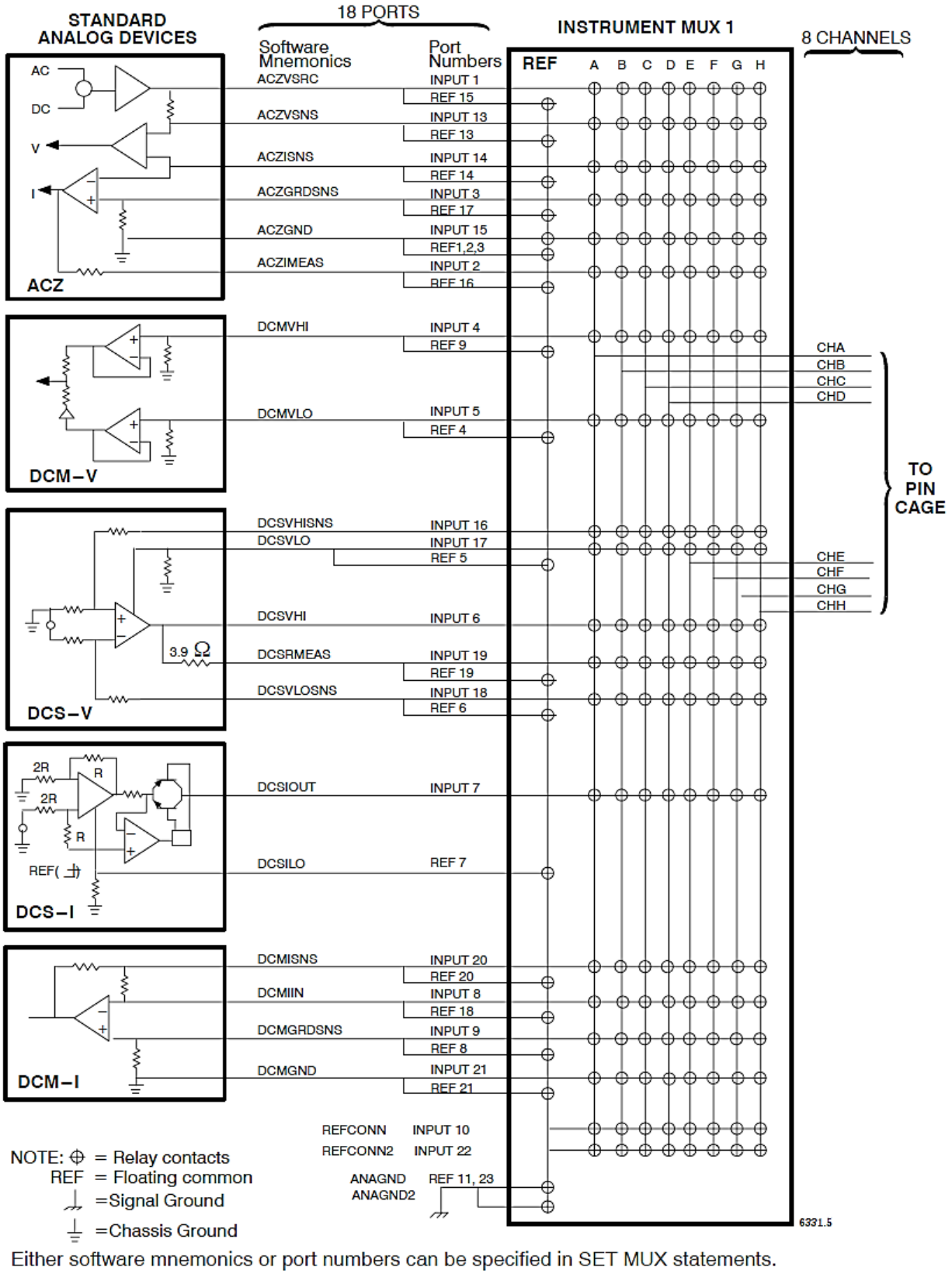
Supp. II 1ST part of schematic circuit – Channel 2



Supp. III2[ND] part of schematic circuit – Channel 1

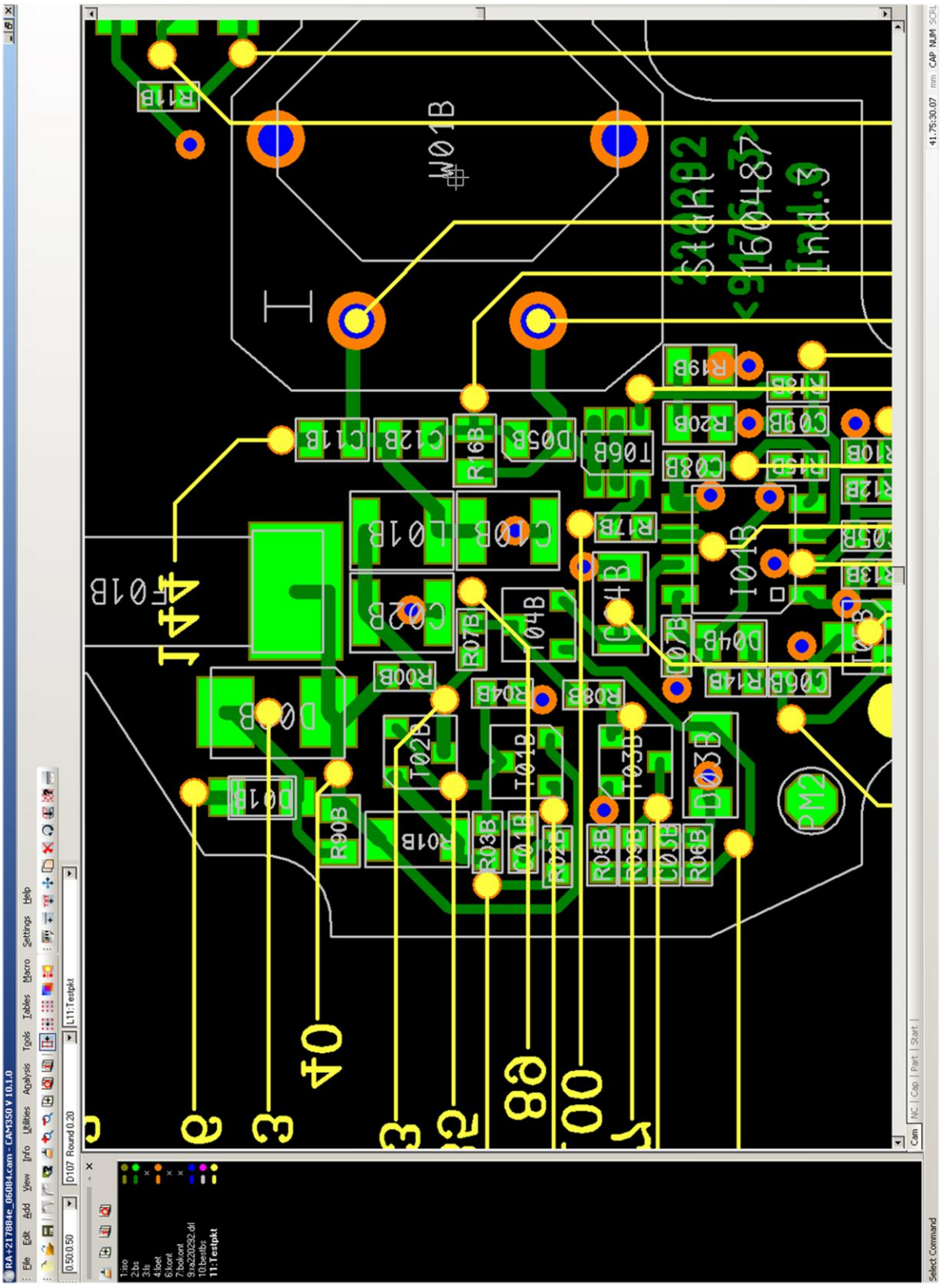


Supp. IV *2ND part of schematic circuit – Channel 2*

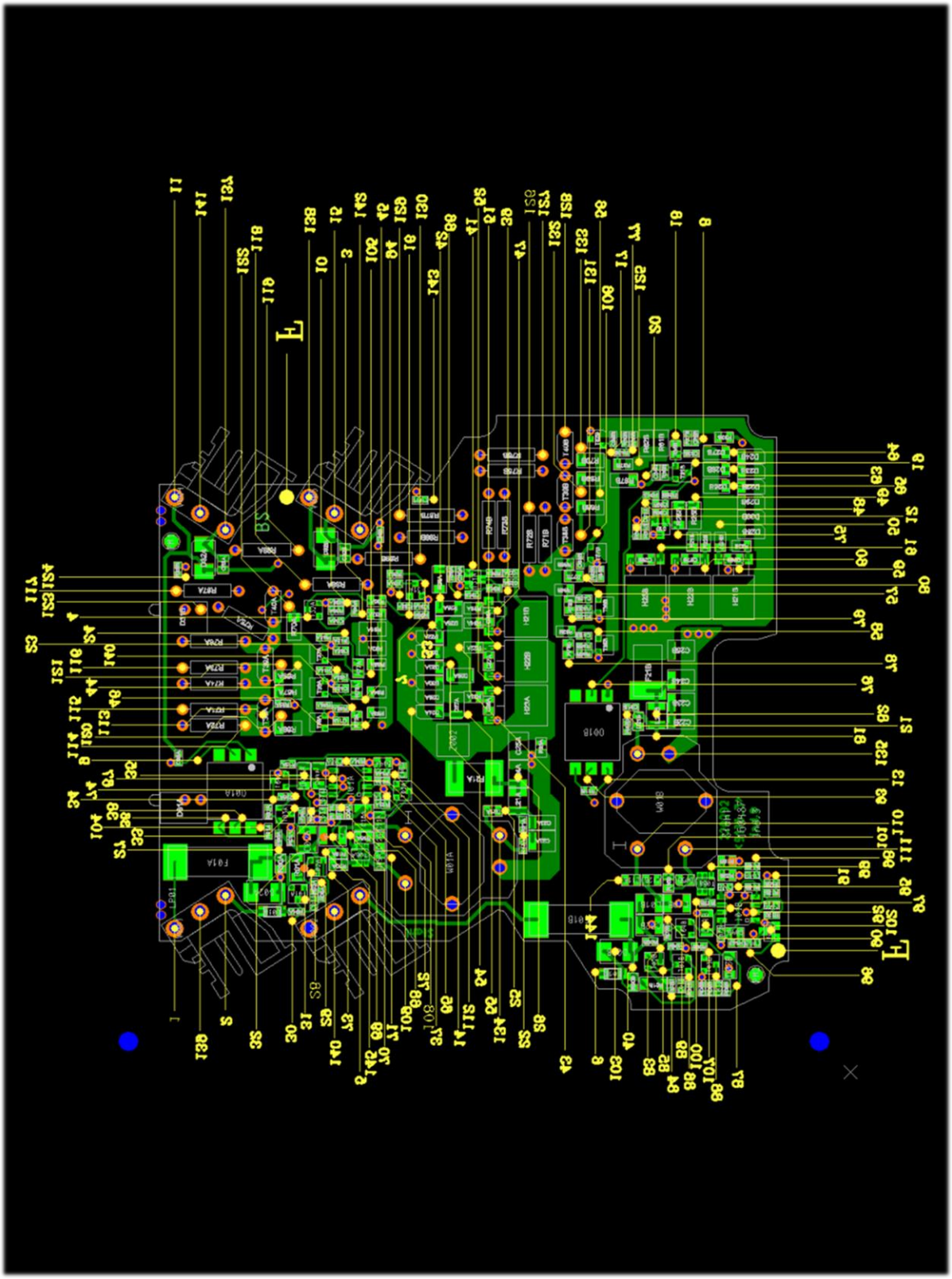


Either software mnemonics or port numbers can be specified in SET MUX statements.

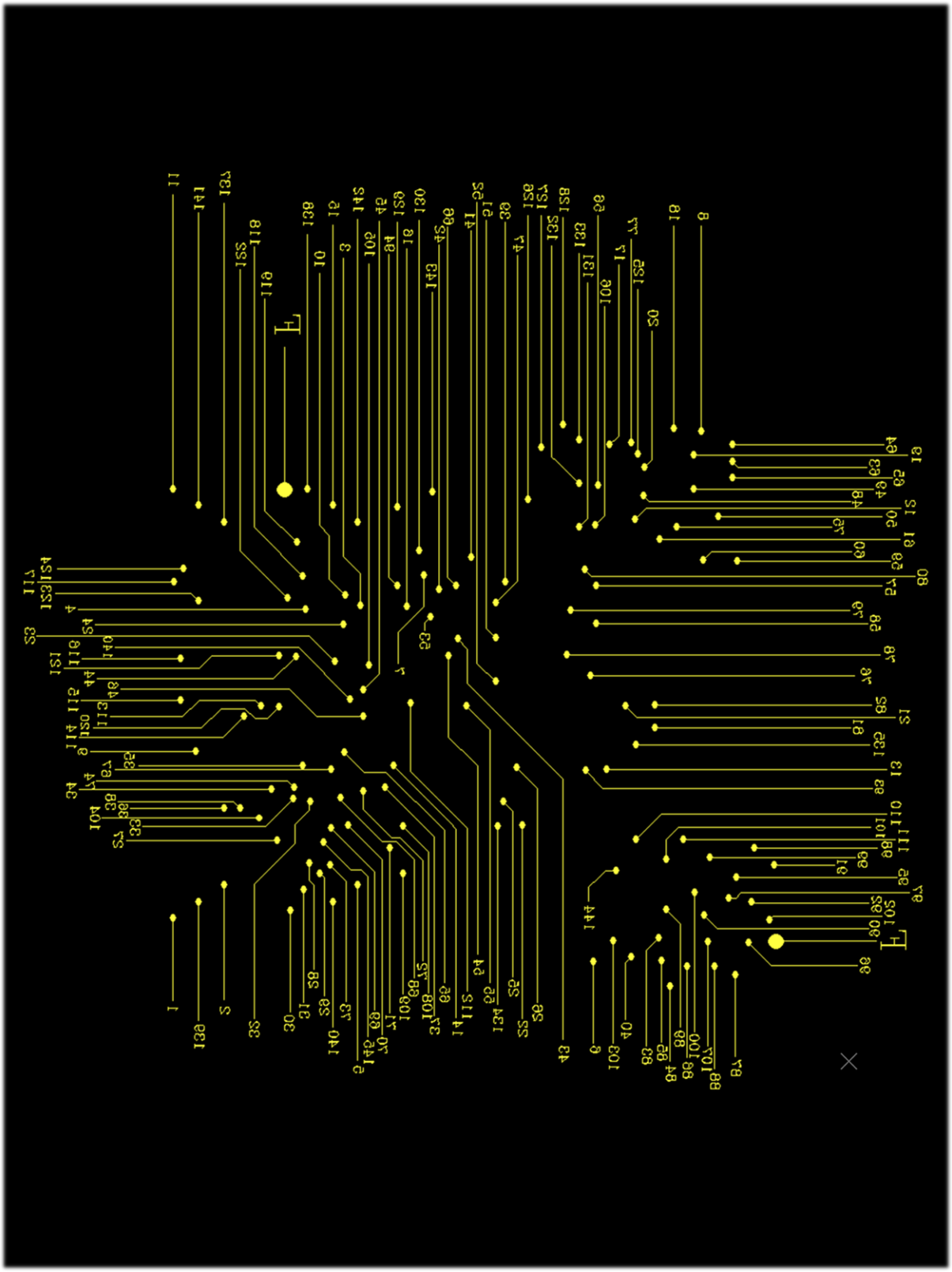
Supp. V Mux and sources/sensors scheme of GenRad™ test machine [3][5]



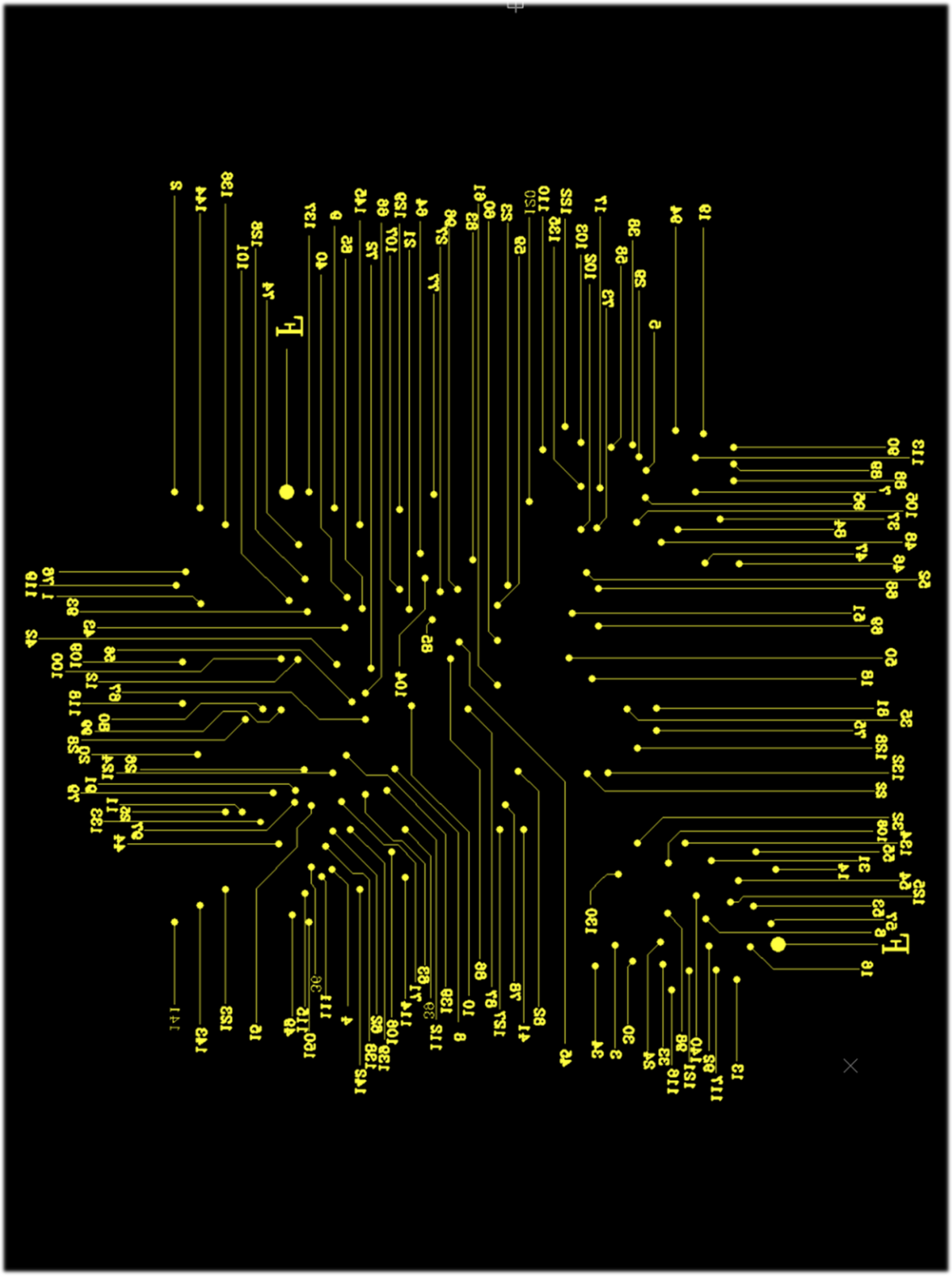
Supp. VI Naming of the nets and placing test flashes



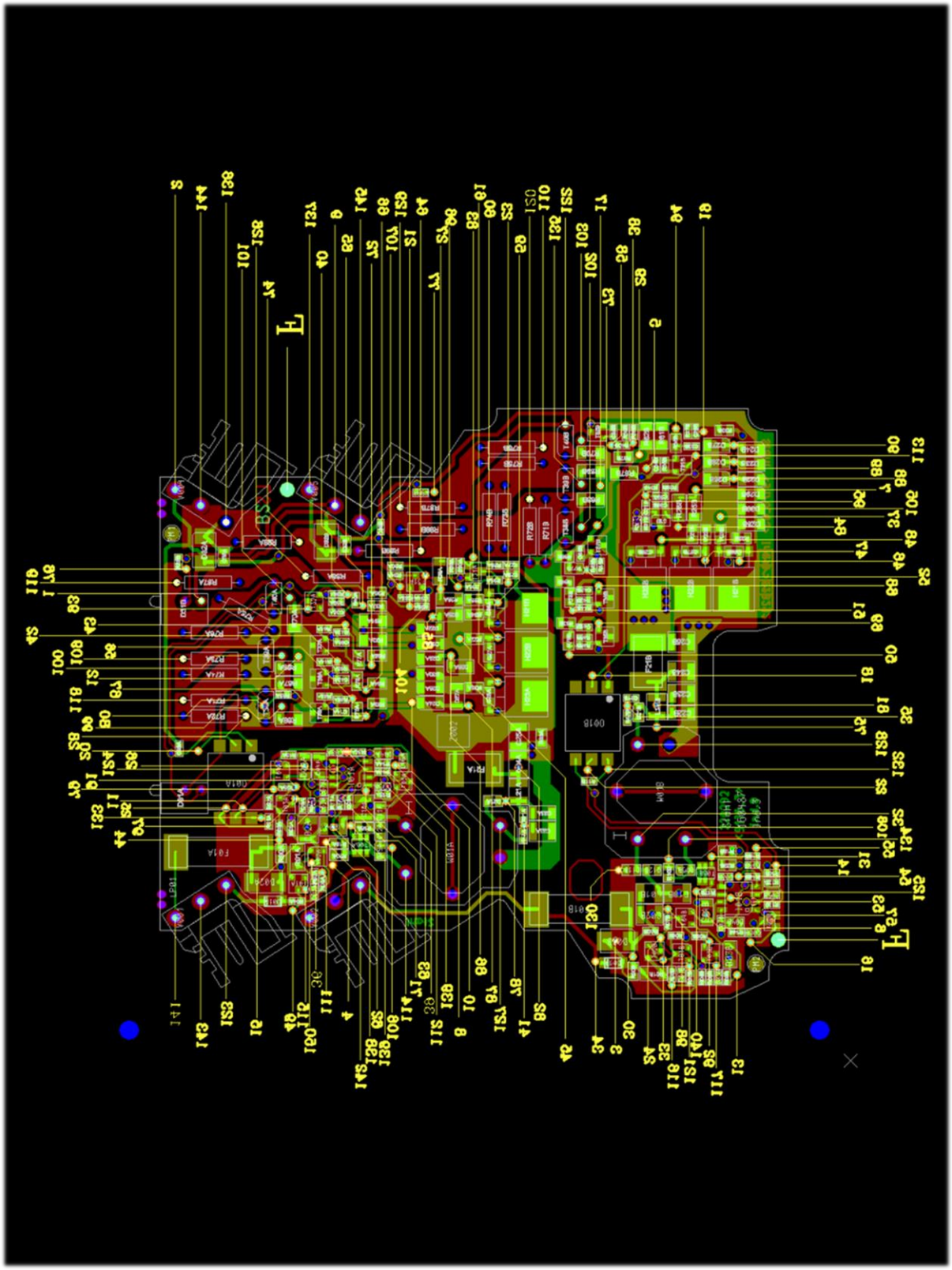
Supp. VII CAD design of PCB with BOT side and temp. numbering of nets



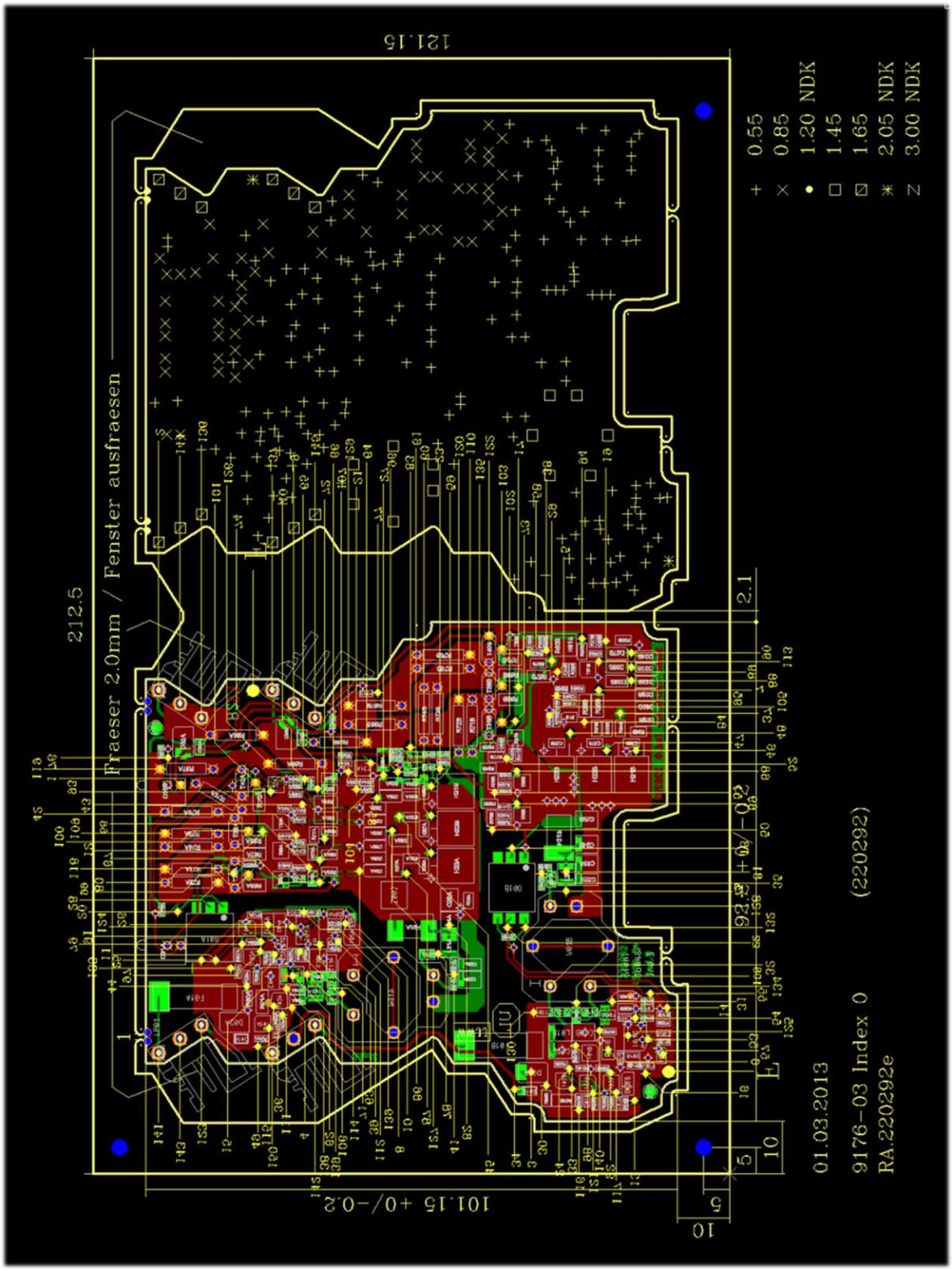
Supp. VIII Net of temporary nails



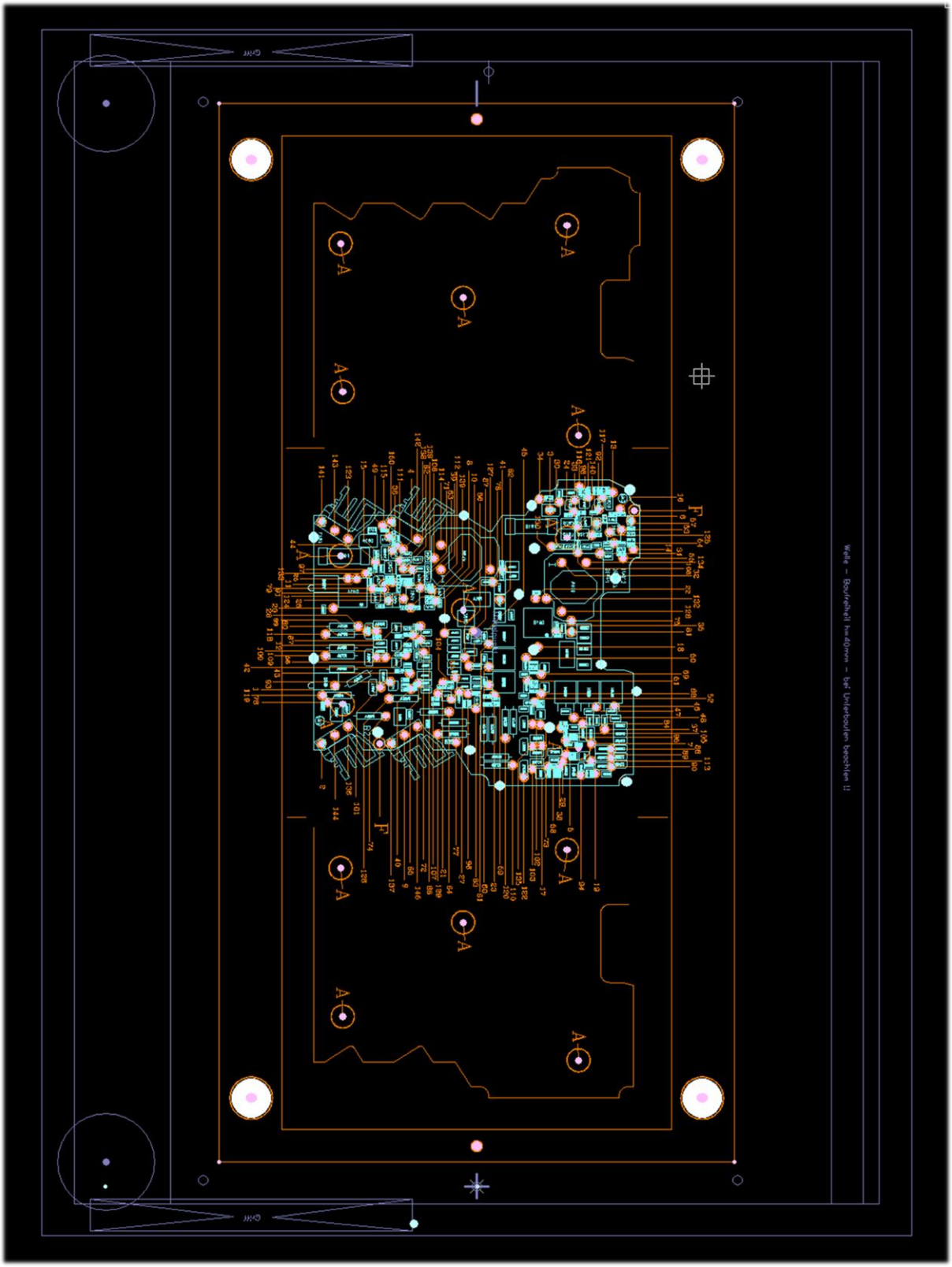
Supp. IXNet of permanent nails



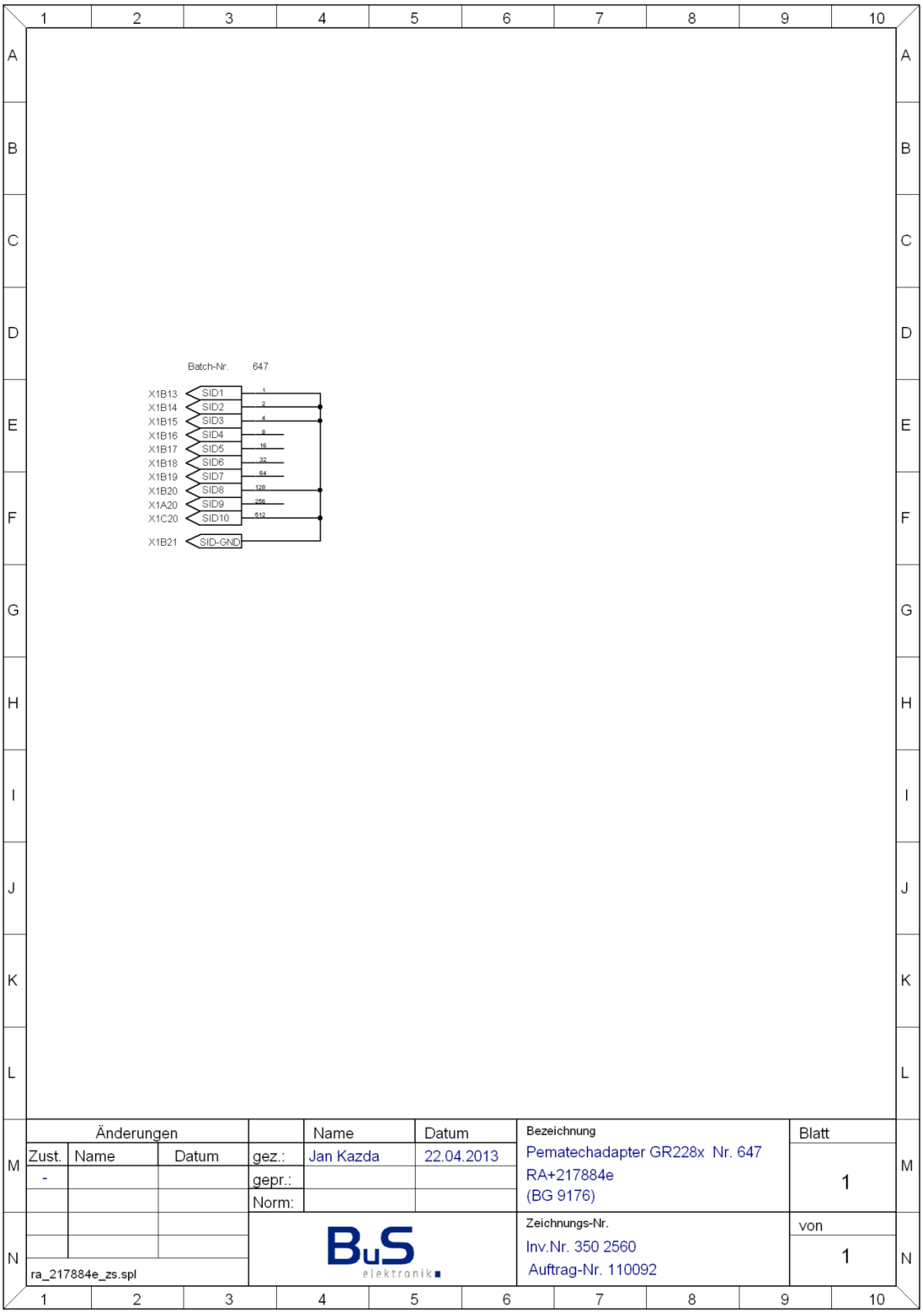
Supp. X CAD design of PCB with both layers and perm. nets numbering



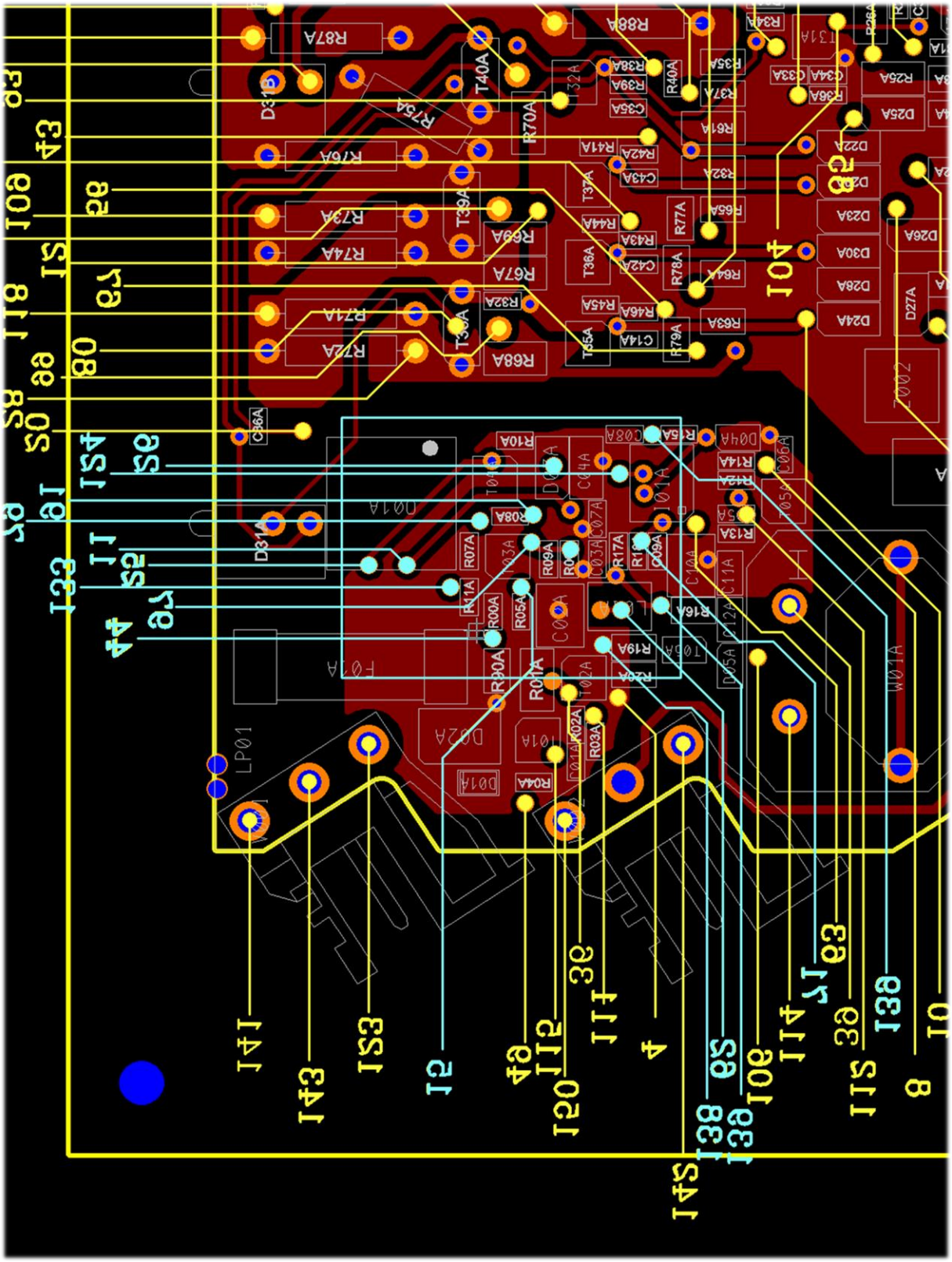
Supp. XIComplete view at CAD design of PCB



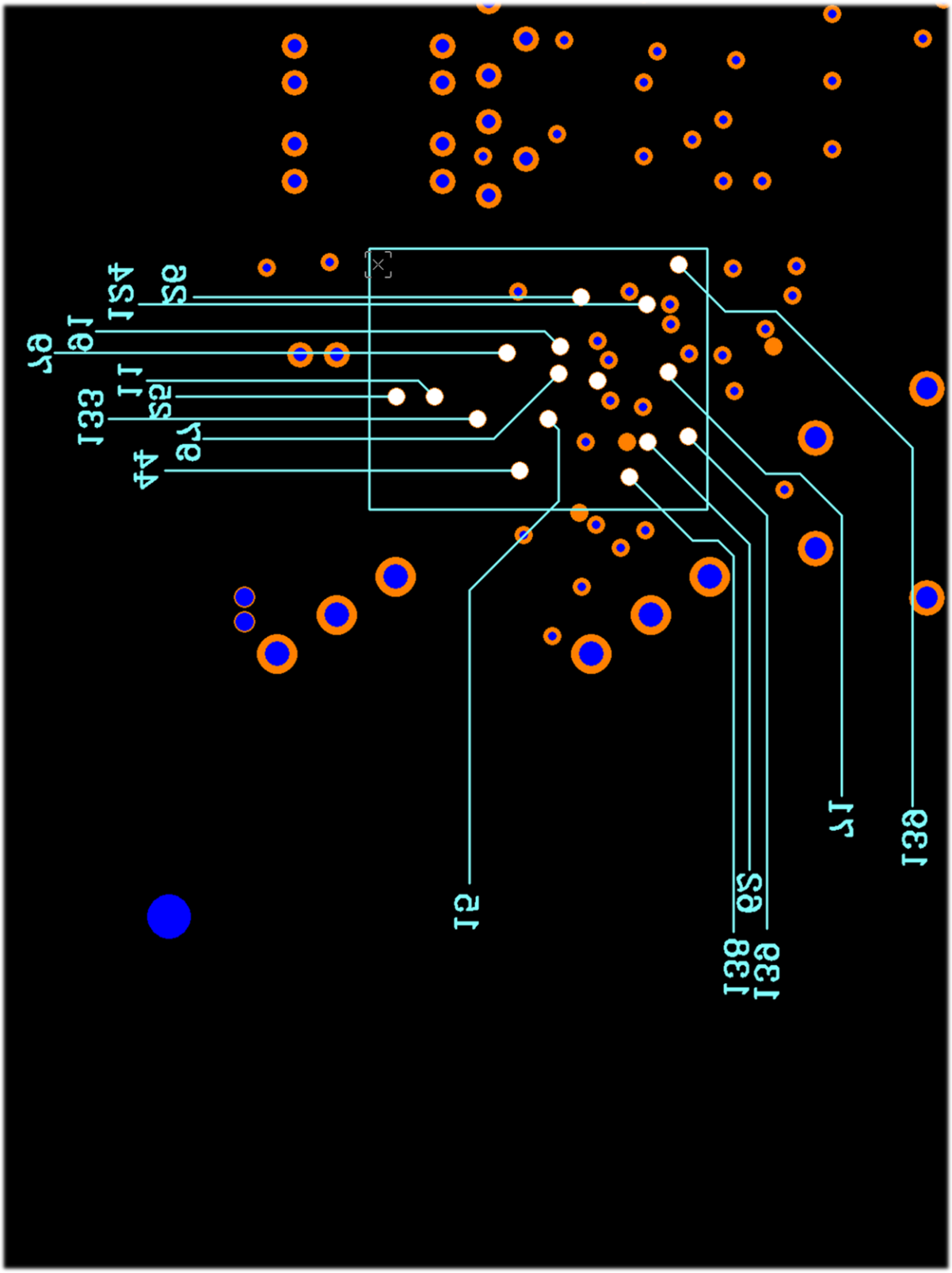
Supp. XII CAD design of permatech adaptor with testing PCB in the middle



Supp. XIII Document to wiring serial number at fixture



Supp. XIV Repairing of missing pin on fixture



Supp. XV Repairing of missing pin on fixture – clear view

Bus Elektronik GmbH & Co. KG
- Confidential -

Request TPT 130418

BuS elektronik
Erstanfrage

Test engineering evaluation of PCBs

Date:	23.04.2013				
Company:	EXAMPLE				
Model:	EAP0276G90A HW+0276G90A:ER				
Annual quantity:	250 Pieces	Lot size:	50 Piece		

EAP3032ATC44 **Circuit programming before placement**

			Group	Hourly		Price
Setup time per item:	10	min	P3/3	30,00 €	**Set-up costs:** (per Loss)	5,00 €
			Gruppe	Hourly		Price
Programming time:	1	min	P3/3	30,00 €	**Programming costs:** (per IC)	0,51 €
Adapter or base:					Initial costs:	

Time required from order placement and delivery of complete and current documentation: 0 working days

Sample availability:	
Procurement Adapter or base:	-----
IC Program creation:	0 AT
IC program verification:	0 AT
IC program handover to FPF:	0 AT

The following documents were missing are for the request and must be in order with current revision:
Programming instructions **Program file**

Flying Probe with test tystem

			Group	Hourly		Price
Setup time per item:	10	min	P2/1	65,00 €	**Set-up costs:** (per Loss)	
			Group	Hourly	Utility values	Price
Test time:	0,0	min	P2/1	65,00 €	0,00 min	0,00 €
Time fault location:	0,0	min	P2/1	65,00 €	0,00 min	0,00 €
Repair time:	0,0	min	P2/4	43,00 €	0,00 min	0,00 €
Number of solder joints + components		Error rate	100	ppm	**Testing costs:** (per panel)	0,00 €
Fault location share:	0,00	%			**Testing costs:** (per unit)	
Test program:					Initial costs:	
Adapter:					Initial costs:	

Time required from order placement and delivery of complete and current documentation: 0 working days

Sample availability:	
Flying Probe treatment:	0 AT
Flying probe drilling program (ELP):	0 AT
Flying probe adapter drill (GMW):	0 AT
Build flying probe adapter:	0 AT
Flying probe calibration:	0 AT
Flying probe MSA creating:	-----
Flying probe handed over to FPF:	0 AT

The following documents were missing are for the request and must be in order with current revision:
BOM **CAD Data** **Cicruit diagram** **Occupancy**

ICT with Test system GR228X

			Group	Hourly		Kosten
Setup time per item:	10	min	P2/2	50,00 €	**Set-up costs:** (per Loss)	8,33 €
			Group	Hourly	Utility values	Kosten
Test time im Nutzen:	0,94	min	P3/2	38,00 €	1,07 min	0,676 €
Time fault location:	2,00	min	P2/2	50,00 €	0,26 min	0,217 €
Repair time:	2,50	min	P2/4	43,00 €	0,33 min	0,233 €
Number of solder joints + components	600	Error rate	200	ppm	**Testing costs:** (per panel)	1,125 €
Fault location share:	12,00	%			**Testing costs:** (per unit)	1,125 €
Test program:					Initial costs:	2.290 €
Pematech adapter with 185 Nails:					Initial costs:	1.750 €

Time required from order placement and delivery of complete and current documentation: 20 working days

Sample availability:	
ICT treatment:	3 AT
ICT drilling program (ELP):	2 AT
ICT Adapter drilling (GMW):	2 AT
ICT Adapter building:	6 AT
ICT Calibrating:	6 AT
ICT MSA create:	-----

Supp. XVI Calculation – part 1

Bus Elektronik GmbH & Co. KG
- Confidential -

Request TPT 130418

BuS elektronik
Erstanfrage

Test engineering evaluation of PCBs

Date:	23.04.2013				
Company:	EXAMPLE				
Model:	EAP0276G90A HW+0276G90A:ER				
Annual quantity:	250	Pieces	Lot size:	50	Piece

ICT handover to FPF: 1 AT

The following documents were missing are for the request and must be in order with current revision:
BOM CAD Data Cicruit diagram Occupancy

HV-Test with Test system

			Group	Hourly		Price
Setup time per item:	10	min	P1/3	57,00 €	Set-up costs: (per Loss)	

			Group	Hourly	Utility values		Price
Time check:	0,0	min	P1/3	57,00 €	0,00	min	0,00 €
Time fault location:	0,0	min	P1/3	57,00 €	0,00	min	0,00 €
Repair time:	0,0	min	P2/4	43,00 €	0,00	min	0,00 €
					Testing costs: (per panel)		0,00 €
Fault location share:	1	%			Testing costs: (per unit)		
Test program:					Initialkosten:		
Adapter:					Initialkosten:		

Time required from order placement and delivery of complete and current documentation: 0 working days

Sample availability:				
HV treatment:	0 AT			
HV drilling program (ELP):	-----			
HV Adapter drilling (GMW):		-----		
HV Adapter building:			0 AT	
HV Calibrating:				0 AT
HV handover to FPF:				0 AT

The following documents were missing are for the request and must be in order with current revision:
Test instructions HV CAD Data Cicruit diagram Occupancy

Functionality test with Test system

			Group	Hourly		Price
Setup time per item:	10	min	P2/3	45,00 €	Set-up costs: (per Loss)	

			Group	Hourly	Utility values		Price
Time check:	0,00	min	P2/3	45,00 €	0,00	min	0,000 €
Time fault location:	0,00	min	P2/3	45,00 €	0,00	min	0,000 €
Repair time:	0,00	min	P2/4	43,00 €	0,00	min	0,000 €
Number of solder joints + components	600	Error rate	100	ppm	Testing costs: (per panel)		0,000 €
Fault location share:	6,00	%			Testing costs: (per unit)		
Test program:					Initialkosten:		
Adapter:					Initialkosten:		
Measuring and testing instruments:					Investition:		

Time required from order placement and delivery of complete and current documentation: 0 working days

Sample availability:				
FKT treatment:	0 AT			
FKT drilling program (ELP):	-----			
FKT Adapter drilling (GMW):		-----		
FKT Adapter building:			-----	
FKT Calibrating:				0 AT
FKT MSA creating:				-----
FKT handover to FPF:				0 AT

The following documents were missing are for the request and must be in order with current revision:
Test instructions FKT CAD Data Cicruit diagram Occupancy

Functionality test 2 with Test system

			Group	Hourly		Price
Setup time per item:	10	min	P2/3	45,00 €	Set-up costs: (per Loss)	

			Group	Hourly	Utility values		Price
Time check:	0,00	min	P2/3	45,00 €	0,00	min	0,000 €
Time fault location:	0,00	min	P2/3	45,00 €	0,00	min	0,000 €

Supp. XVII Calculation – part 2

Bus Elektronik GmbH & Co. KG
- Confidential -

Request **TPT** **130418**

BuS elektronik

Erstanfrage

Test engineering evaluation of PCBs

Date:	23.04.2013							
Company:	EXAMPLE							
Model:	EAP0276G90A HW+0276G90A:ER							
Annual quantity:	250	Pieces		Lot size:	50	Piece		
Repair time:	0,00	min	P2/4	43,00 €		0,00	min	0,000 €
Number of solder joints + components	600	Error rate	100	ppm		**Testing costs:** (per panel)		0,000 €
Fault location share:	6,00	%				**Testing costs:** (per unit)		
Test program:						Initialkosten:		
Adapter:						Initialkosten:		
Measuring and testing instruments:						Investition:		

Time required from order placement and delivery of complete and current documentation: 0 working days

Sample availability:				
FKT2 treatment:	0 AT			
FKT2 drilling program (ELP):	-----			
FKT2 Adapter drilling (GMW):		-----		
FKT2 Adapter building:			-----	
FKT2 Calibrating:				0 AT
FKT2 MSA creating:				-----
FKT2 handover to FPF:				0 AT

The following documents were missing are for the request and must be in order with current revision:
Test instructions FKT **CAD Data** **Cicruit diagram** **Occupancy**

Funcionality test 3 with Test system

			Group	Hourly			Price
Setup time per item:	10	min	P2/3	45,00 €	**Set-up costs:** (per Loss)		
			Group	**Hourly**	**Utility values**		**Price**
Time check:	0,00	min	P2/3	45,00 €	0,00	min	0,000 €
Time fault location:	0,00	min	P2/3	45,00 €	0,00	min	0,000 €
Repair time:	0,00	min	P2/4	43,00 €	0,00	min	0,000 €
Number of solder joints + components	600	Error rate	100	ppm	**Testing costs:** (per panel)		0,000 €
Fault location share:	6,00	%			**Testing costs:** (per unit)		
Test program:					Initialkosten:		
Adapter:					Initialkosten:		
Measuring and testing instruments:					Investition:		

Time required from order placement and delivery of complete and current documentation: 0 working days

Sample availability:				
FKT3 treatment:	0 AT			
FKT3 drilling program (ELP):	-----			
FKT3 Adapter drilling (GMW):		-----		
FKT3 Adapter building:			-----	
FKT3 Calibrating:				0 AT
FKT3 MSA creating:				-----
FKT3 handover to FPF:				0 AT

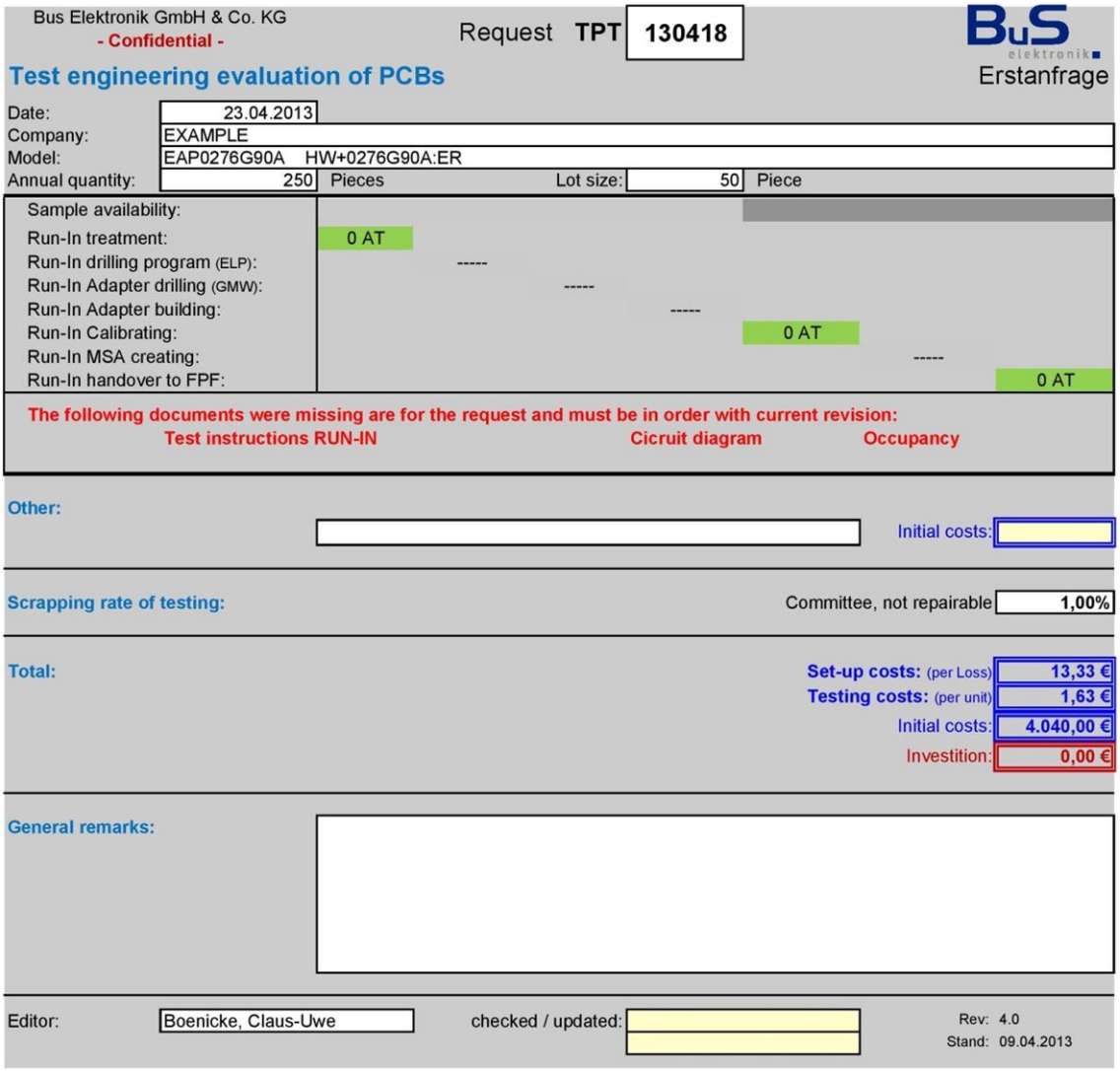
The following documents were missing are for the request and must be in order with current revision:
Test instructions FKT **CAD Data** **Cicruit diagram** **Occupancy**

0h Run-In with oven

			Group	Hourly			Price
Setup time per item:	15	min	P3/3	30,00 €	**Set-up costs:** (per Loss)		
			Group	**Hourly**	**Utility values**		**Price**
Time samples populate:	0,00	min	P3/3	30,00 €	0,00	min	0,00 €
Time duration of test:	0,00	min	P5/3	2,22 €	0,00	min	0,00 €
Time fault location:	0,0	min	P1/3	57,00 €	0,00	min	0,00 €
Repair time:	0,0	min	P2/4	43,00 €	0,00	min	0,00 €
Energy consumption of test station	2	kW	0,22 € / h				
Fault location share:	3	%			**Set-up costs:** (per Loss)		
Test program:					Initialkosten:		
Adapter:					Initialkosten:		
Measuring and testing instruments:					Investition:		

Time required from order placement and delivery of complete and current documentation: 0 working days

Supp. XVIII Calculation – part 3



Bus Elektronik GmbH & Co. KG
- Confidential -

Request TPT 130418

BuS elektronik
Erstanfrage

Test engineering evaluation of PCBs

Date:	23.04.2013				
Company:	EXAMPLE				
Model:	EAP0276G90A HW+0276G90A:ER				
Annual quantity:	250	Pieces	Lot size:	50	Piece

Sample availability:						
Run-In treatment:	0 AT					
Run-In drilling program (ELP):		-----				
Run-In Adapter drilling (GMW):			-----			
Run-In Adapter building:				-----		
Run-In Calibrating:					0 AT	
Run-In MSA creating:						-----
Run-In handover to FPF:						0 AT

The following documents were missing are for the request and must be in order with current revision:
Test instructions RUN-IN **Cicruit diagram** **Occupancy**

Other:

Initial costs:

Scrapping rate of testing:

Committee, not repairable 1,00%

Total:

Set-up costs: (per Loss) 13,33 €
Testing costs: (per unit) 1,63 €
Initial costs: 4.040,00 €
Investition: 0,00 €

General remarks:

Editor: Boenicke, Claus-Uwe checked / updated:

Rev: 4.0
Stand: 09.04.2013

Supp. XIX Calculation – part 4

Bus Elektronik GmbH Co. KG

Calculation of ICT Test programm

(with Adapter build documentation)

Request Nr.	130418	Date:	23.04.2013
Customer:	EXAMPLE	Editor:	Boenicke, Cla
Model:	EAP0276G90A HW+0276G90A:ER		
Benefit:	1		
Test system:	GR228X		
Programming:			

Documents	Name / File name	Revision	Missing
BOM			X
CAD Data			X
Cicruit diagram			X
Occupancy			X

Stock	Description	E-Price [EUR]	G-Price [EUR]
0	Base price for 150 test points	xxx,xx	
0	Charge for each additional 50 test points	xxx,xx	
0	Measurement points (number of test points)	xxx,xx	
0	Resistors	xxx,xx	
0	Capacitors, Coils	xxx,xx	
0	Diodes	xxx,xx	
0	Z-Diodes, Voltage limiters, LEDs	xxx,xx	
0	Transistors (Bipolar)	xxx,xx	
0	FET´s	xxx,xx	
0	Quartz	xxx,xx	
0	Connectors	xxx,xx	
0	Combinatorial and sequence circuits	xxx,xx	
0	Bus driver and buffer circuits with tri-state outputs	xxx,xx	
0	RAM, EEPROM	xxx,xx	
0	DAC, ADC, PAL	xxx,xx	
0	ROM, EPROM,	xxx,xx	
0	Processors and their periphery	xxx,xx	
0	Operational amplifiers (per amplifier)	xxx,xx	
0	Optocouplers per channel	xxx,xx	
0	Relays	xxx,xx	
0	Power-MOSFET Controller (per output)	xxx,xx	
0	Power-Supply (each output voltage)	xxx,xx	
0	Sensors	xxx,xx	
0	Other	xxx,xx	
0	OpensXpress	xxx,xx	
0	Opens-Dummy´s (Dummy-Burst Disable-Section)	xxx,xx	
0	Frequency/voltage measurement	xxx,xx	
0	Boundary-Scan	xxx,xx	
0 h	Modification of the standard Rohprogrammes (ATO-Integration, Kontaktierungstest, German texts, sequence displays, Entladeroutinen Elko´s, Nutzensteuerung, version control) [in h]	xxx,xx	
0 h	additional manual work in data entry (no CAD data) [in h]	xxx,xx	
	Price of test program:		**0,00**
0 h	Small batch testing [in h]	0,00	0,00
0 h	MSA [in h] ***at Automotive OBLIGATION***		
0 h	Creation of documents (test instructions, test certificate, ...) [in h]	0,00	0,00
0 h	Handover to the production [in h]		
	Total price of test program:		**0**

Supp. XX Calculation of ICT Test program – part 1

Calculation of ICT-Adapter

(adapter without creating documents, used number is entered)

Stock	Description	E-Price [EUR]	G-Price [EUR]
0	*Total number of test points*		
0	Base price project (up to 300 test points)	xxx,xx	
0	Surcharge for each additional 100 test points	xxx,xx	
0	CNC Set-up	xxx,xx	
0	Shorting plate	xxx,xx	
0	Ground plane	xxx,xx	
0	Two-sided contacting *(specifically calculated)*	xxx,xx	
0	*Number of test points on the second side*		
0	Additional circuits *(specifically calculated)*	xxx,xx	
0	2A small simple relay (incl. wiring)	xxx,xx	
0	2A small twin relay (incl. wiring)	xxx,xx	
0	8/16A large simple relay (incl. wiring)	xxx,xx	
0	8/16A large twin relay (incl. wiring)	xxx,xx	
0	Programmer for Processor	xxx,xx	
0	other	xxx,xx	
0	other	xxx,xx	
0	other	xxx,xx	
0	other	xxx,xx	
0	Hold-down pins	xxx,xx	
0	Standard wire (AWG 30)	xxx,xx	
0	Power wire (AWG26)	xxx,xx	
0	Additional charge for Twisted Pair, solder, coax connection	xxx,xx	
0	Spring contact with shell grid 100mil (2.54mm)	xxx,xx	
0	Spring contact with shell grid 75mil (1,90mm)	xxx,xx	
0	Spring contact with shell grid 50mil (1,27mm) *with wire*	xxx,xx	
0	Long stroke spring contact with shell grid 100mil (2,54mm)	xxx,xx	
0	Long stroke spring contact with shell grid (1,90mm)	xxx,xx	
0	Long stroke spring contact with shell grid (1,27mm) *with wire*	xxx,xx	
0	Spring contact with specific shell design *(specifically calculated)*	xxx,xx	
0	Switch contact with shell	xxx,xx	
0	Install hold-down	xxx,xx	
0	Needle drilling 100mil	xxx,xx	
0	Needle drilling 75mil	xxx,xx	
0	Needle drilling 50mil	xxx,xx	
0	Tubes and needles put 100mil	xxx,xx	
0	Tubes and needles put 75mil	xxx,xx	
0	Tubes and needles put 50mil	xxx,xx	
0	Wiring 100mil	xxx,xx	
0	Wiring 75mil	xxx,xx	
0	Wiring 50mil	xxx,xx	
0	Millings per 5cm²	xxx,xx	
0 h	CAD working [in h]	xxx,xx	
0 h	Assembly working [in h]	xxx,xx	
	Pematech exchange use		
0	**Base price of adapter (315x210 without needles, including guide pins, top)**	xxx,xx	
0	Charge guide ball bearing 11mm	xxx,xx	
0	additional guide pin	xxx,xx	
0	additional support suspension 6mm	xxx,xx	
0	Snapper (LP bracket)	xxx,xx	
0	Eccentric	xxx,xx	
0	Lift	xxx,xx	
0	Needle guide plate (100x100 without needles, including guide pins)	xxx,xx	
0	Needle guide plate (150x100 without needles, including guide pins)	xxx,xx	
0	Needle guide plate (150x150 without needels, including guide pins)	xxx,xx	
0	Needle guide plate (200x150 without needles, including guide pins)	xxx,xx	
0	Needle guide plate (200x200 without needles, including guide pins)	xxx,xx	
0	Needle guide plate (250x200 without needles, including guide pins)	xxx,xx	
0	Double contacting *(specifically calculated)*	xxx,xx	
	ATX exchange use		
0	**Base price of adapter (Nutzfl. 410x260 - 450 needles)**	xxx,xx	
0	ATX Pin	xxx,xx	
0	Additional guide pin	xxx,xx	
0	Mounting base price of ATX Adapter	xxx,xx	
0	Put ATX pin	xxx,xx	
	TECO MSW600 (only for two-sided contacting)		

Supp. XXI Calculation of ICT Test program – part 2

0	**Base price of adapter**	xxx,xx	
0	Base price by mounting TECO adapter	xxx,xx	
	Vacuum adapter		
0	**Adapter TECO N2 228x (without needles 290x310)**	xxx,xx	
0	**Adapter TECO N3 228x (without needles 550x580)**	xxx,xx	
0	**Adapter Ingun VA2040 228x to 1536 TP (without needles 430x310)**	xxx,xx	
0	**Adapter Ingun VA2040 228x to 1536 TP two-staged (without needles 390x310)**	xxx,xx	
0	TECO Interface for 640 TP (Slot 0-8+AFTM)	xxx,xx	
0	TECO Interface for 896 TP (Slot 0-10+AFTM)	xxx,xx	
0	TECO Interface for 1152 TP (Slot 0-12+AFTM)	xxx,xx	
0	TECO Interface for 1536 TP (Slot 0-15)	xxx,xx	
0	Vacuum hood 120x170x55 (100x150x10 without needl., including retainer and gasket)	xxx,xx	
0	Vacuum hood 180x250x55 (160x230x10 without needl., including retainer and gasket)	xxx,xx	
0	Vacuum hood 200x300x55 (180x280x10 without needl., including retainer and gasket)	xxx,xx	
0	Vacuum hood 220x360x55 (200x340x10 without needl., including retainer and gasket)	xxx,xx	
0	Vacuum hood 300x360x55 (280x340x10 without needl., including retainer and gasket)	xxx,xx	
0	Vacuum hood 315x385x55 (295x365x10 without needl., including retainer and gasket)	xxx,xx	
0	Vacuum hood 300x360x75 (280x340x10 without needl., including retainer and gasket)	xxx,xx	
0	Waterproofing construction group-specific	xxx,xx	
0	Base price by mounting vacuum adapter	xxx,xx	
0	Performance of waterproofing construction group-specific	xxx,xx	
	Creating external adapter (Offer)		
0	Attachments *(specifically calculated)*	xxx,xx	
0	Programmer *(specifically calculated)*	xxx,xx	
0	Check sign stamper	xxx,xx	

Total price of material:	**0,00**
Total price of performance:	**0,00**

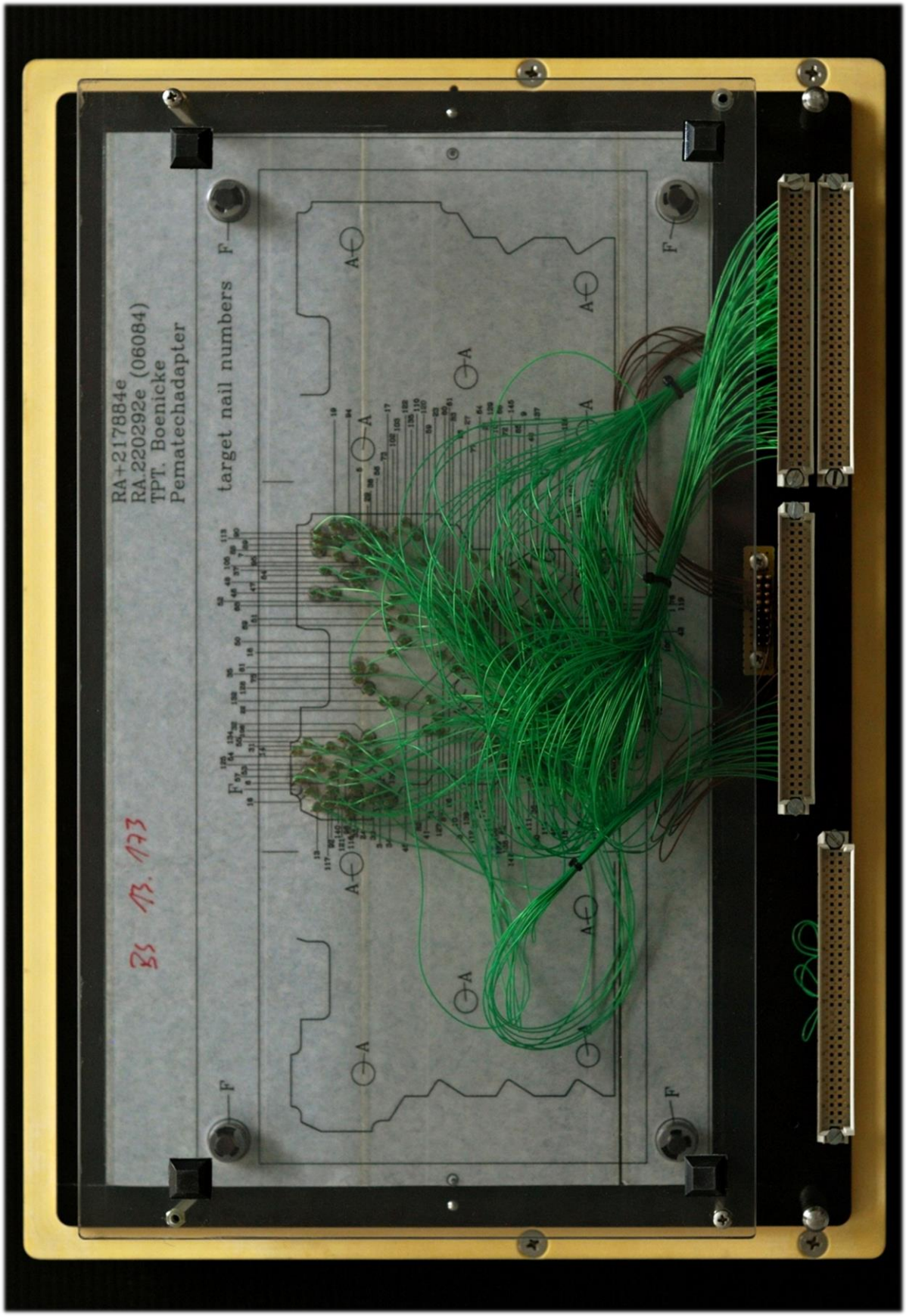
Number of necessary adaptors		
0	**Total price of adaptors:**	**0**

Cost of ICT inspection time

Stock	Description	Time unit [s]	Total [s]
0	Benefit		
0	Time for insertion of the BG / benefit of the adapter	1	
0	Time for taking out the BG / benefit of the adapter	1	
0	Time stamps (total time for all boards)	1	
0	Other work (Total time for all boards)	1	
0	Time programming (programming on one board)	1	
0	Test time (Program running time for a board)	1	
	Summe		***0,00***
3%	with pseudo-error component, other running costs		0,00
	Total time		**0,00**
	Testing time per BG		

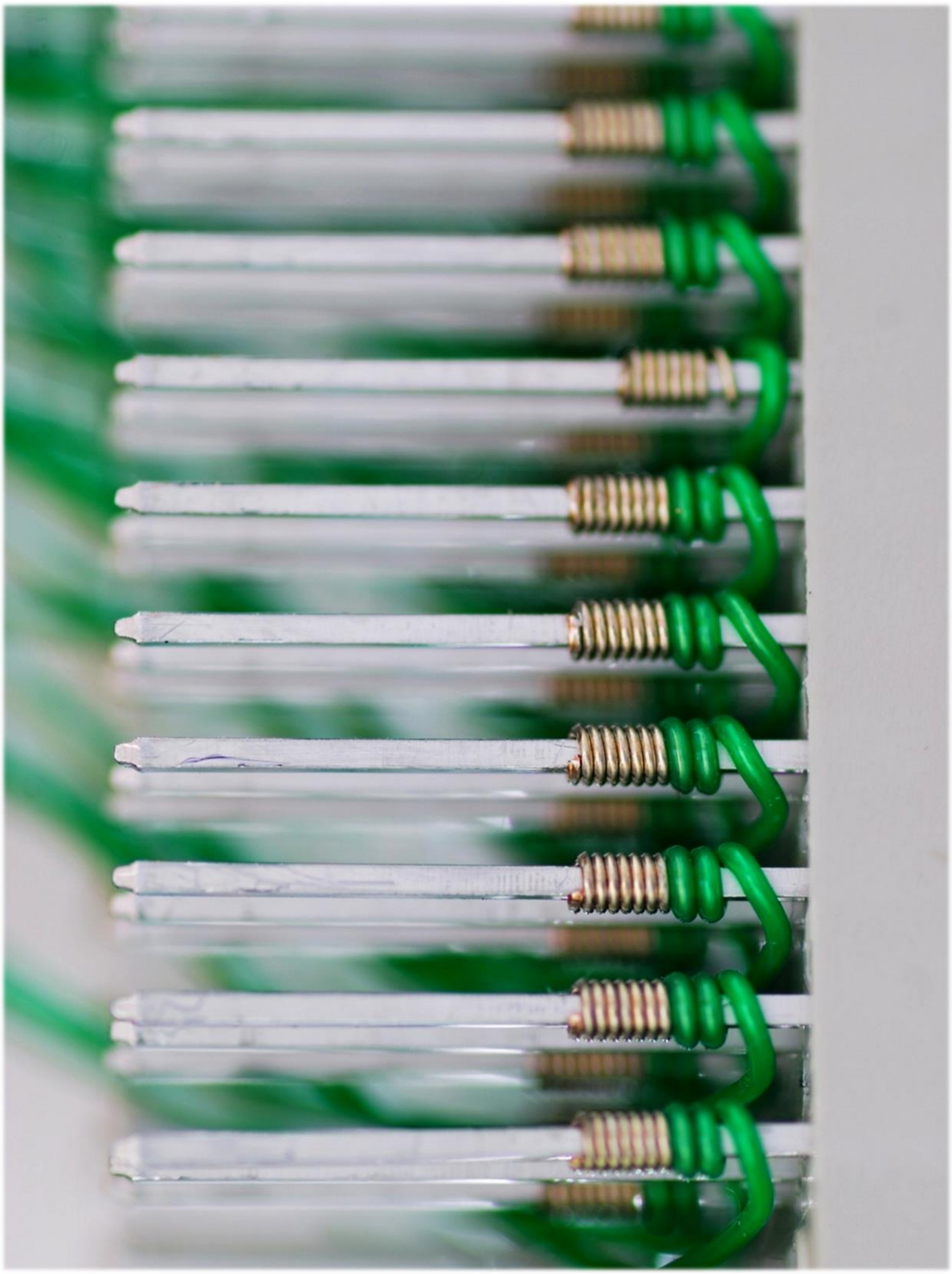
Supp. XXII Calculation of ICT Test program – part 3

Supp. XXIII Fixture from the top without placed PCB



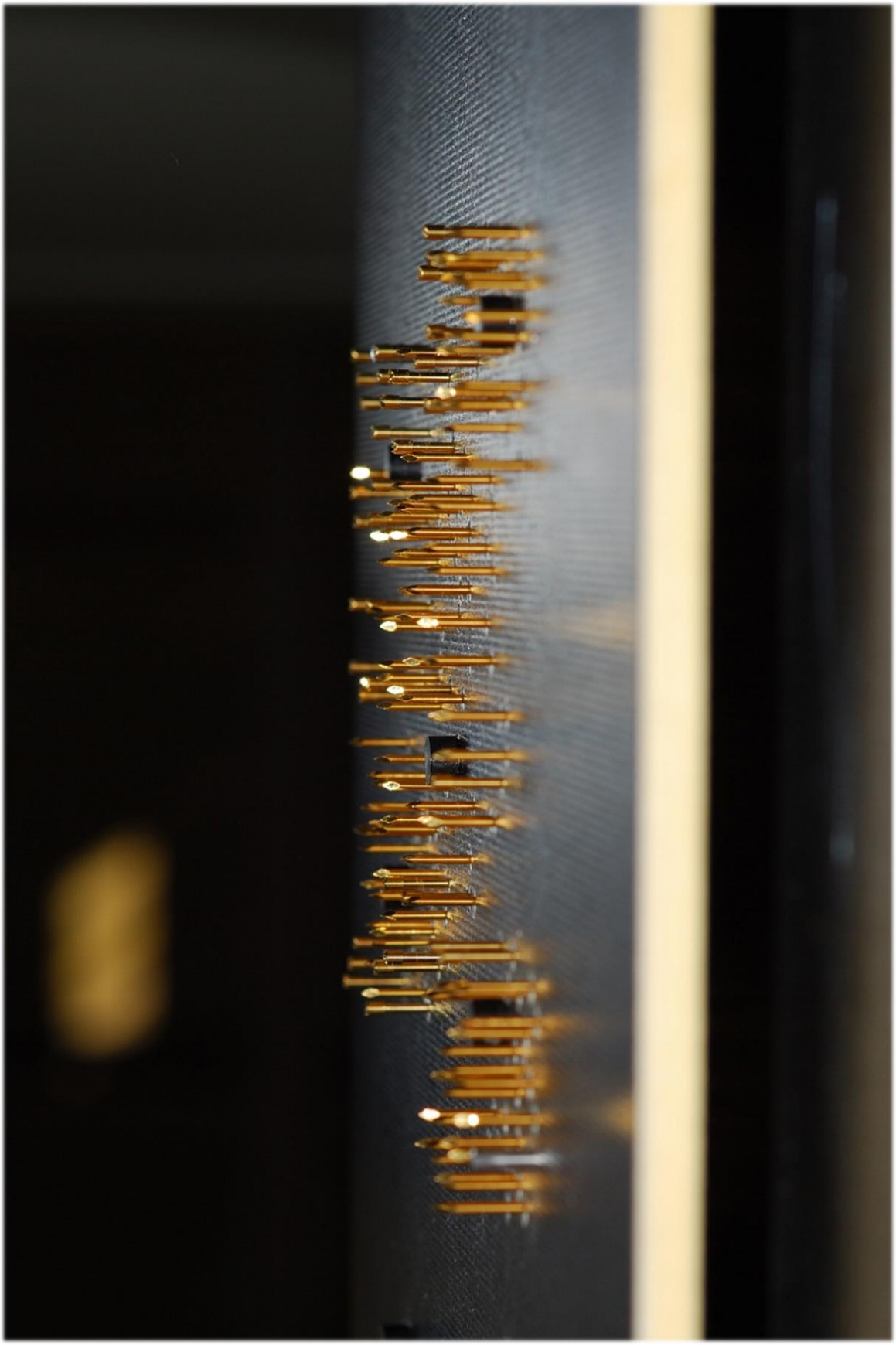
Supp. XXIV Fixture from the bottom and wires

Supp. XXV Fixture from the top with placed PCB

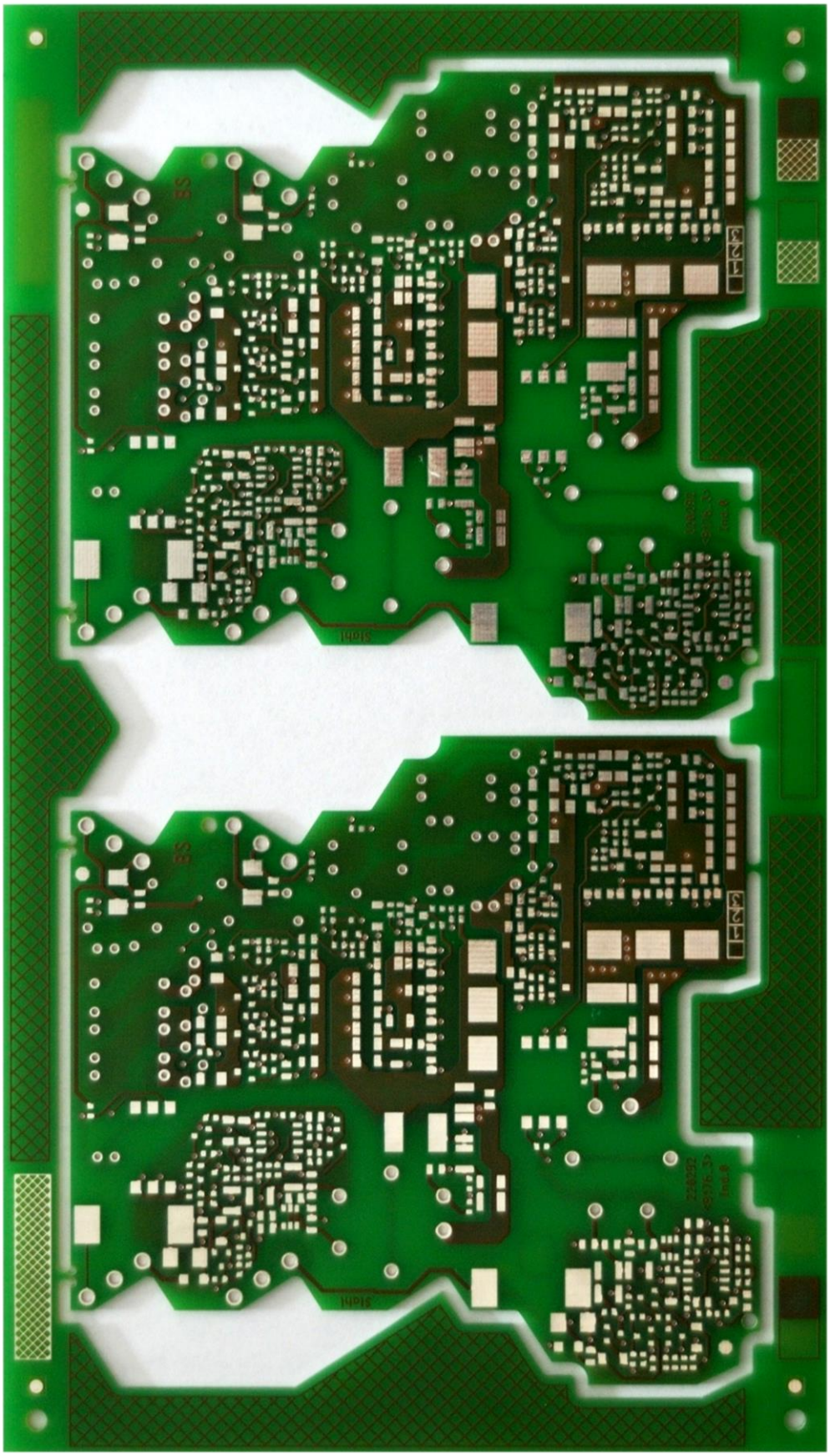


Supp. XXVI Detail of wiring the wires to the connector

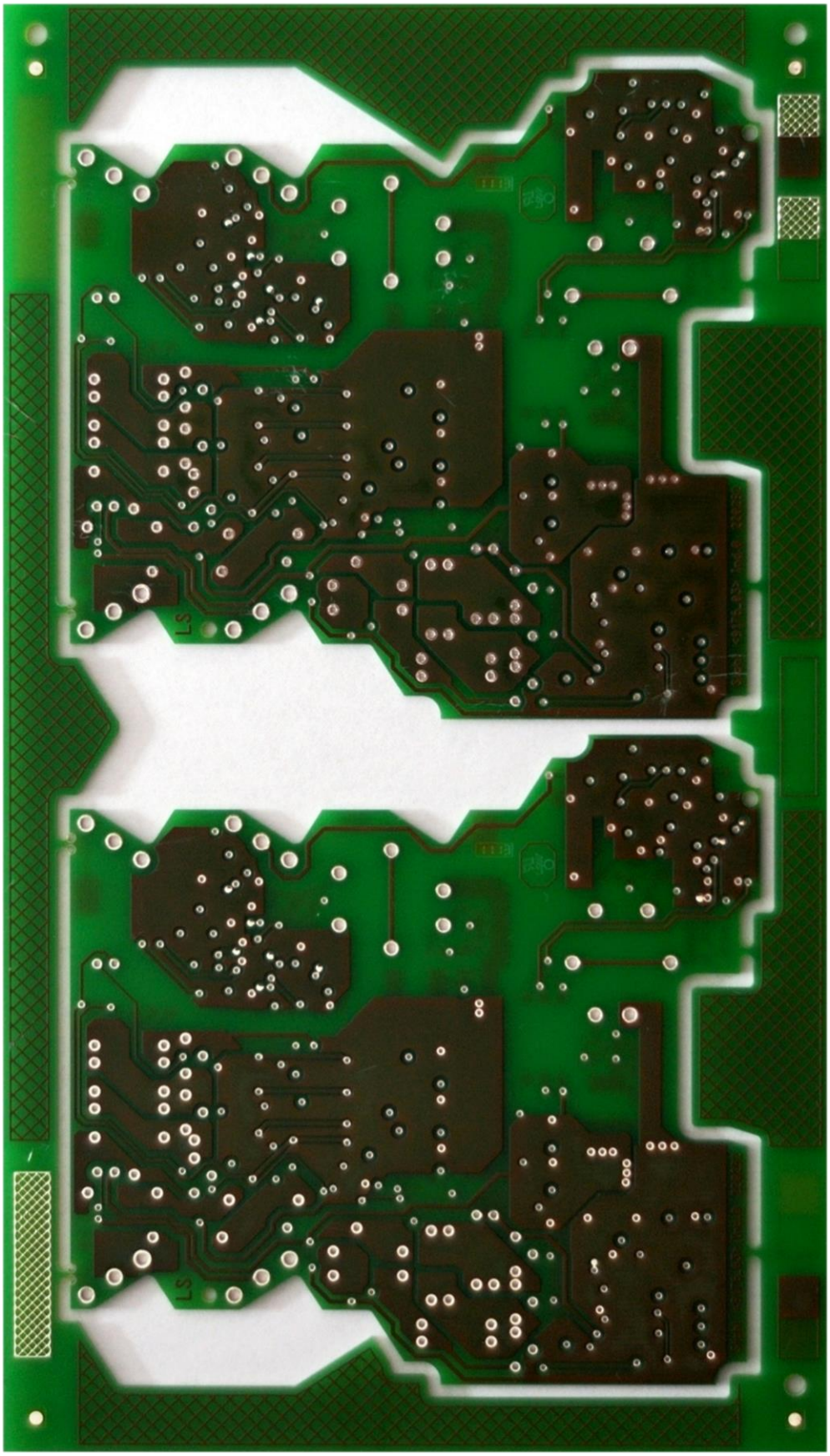
Supp. XXVII Detail at mounted connectors on the fixture



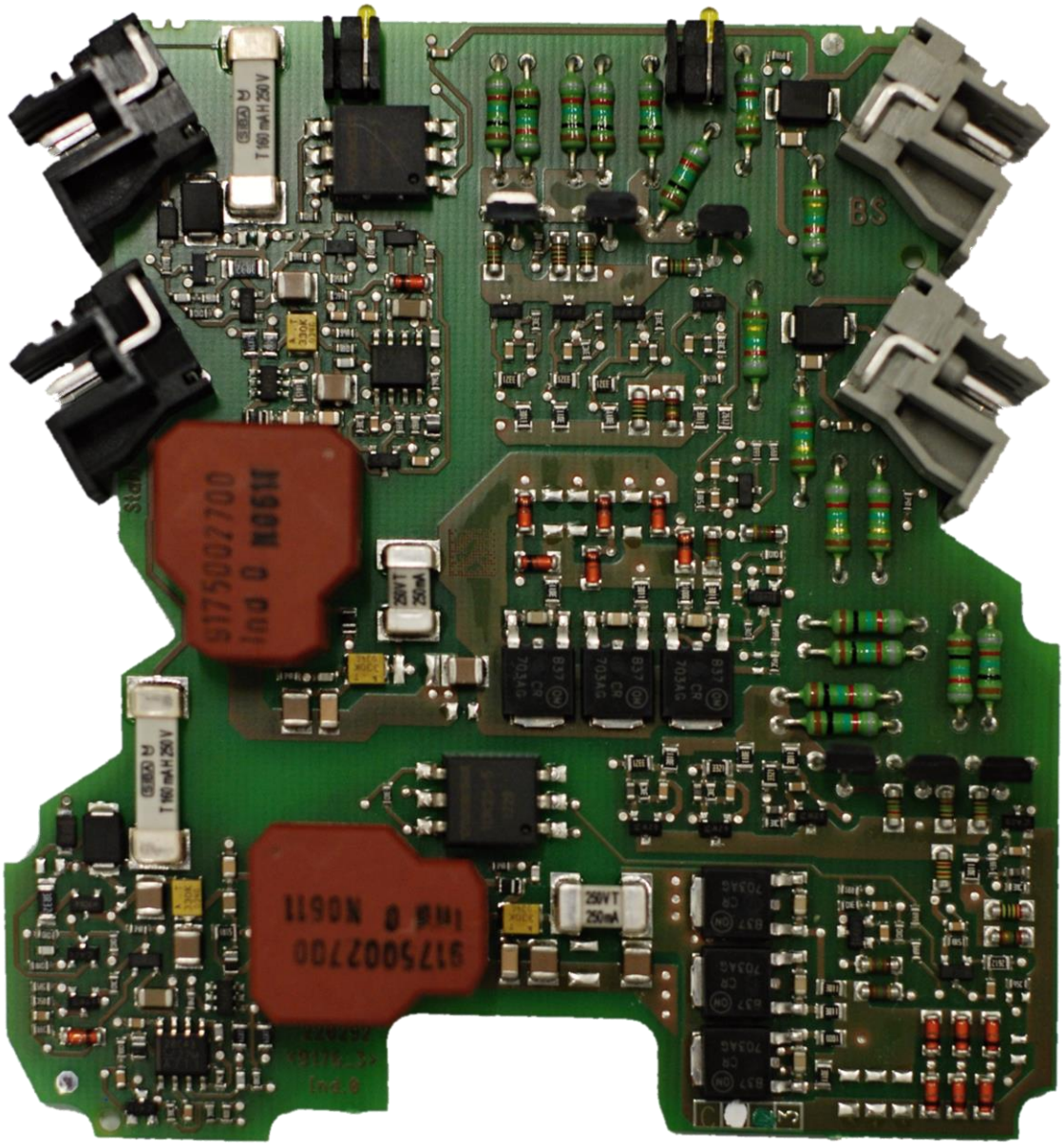
Supp. XXVIII Detail of the testing nails with pull down top desk



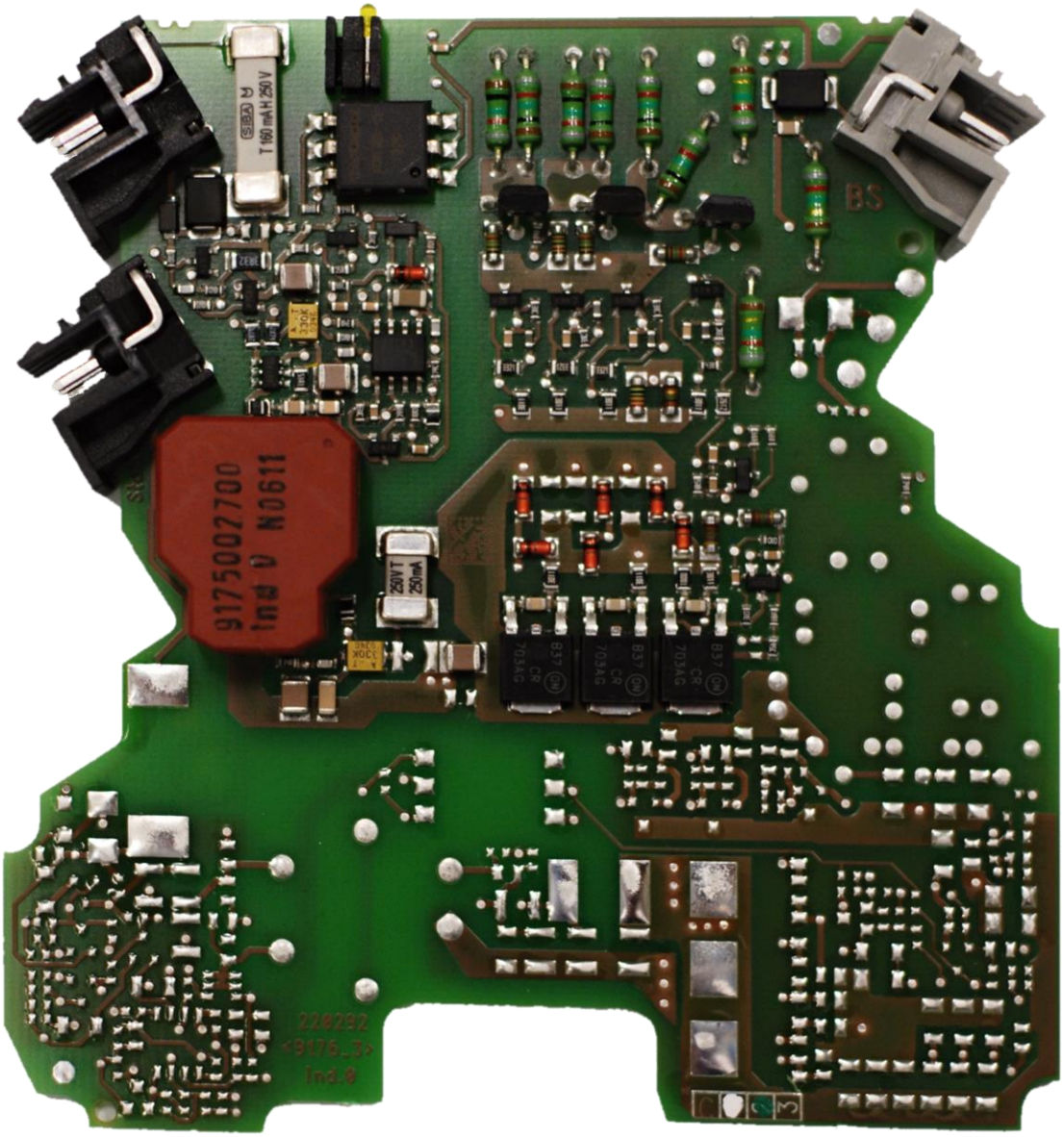
Supp. XXIX Unassembled printed circuit board from bottom side



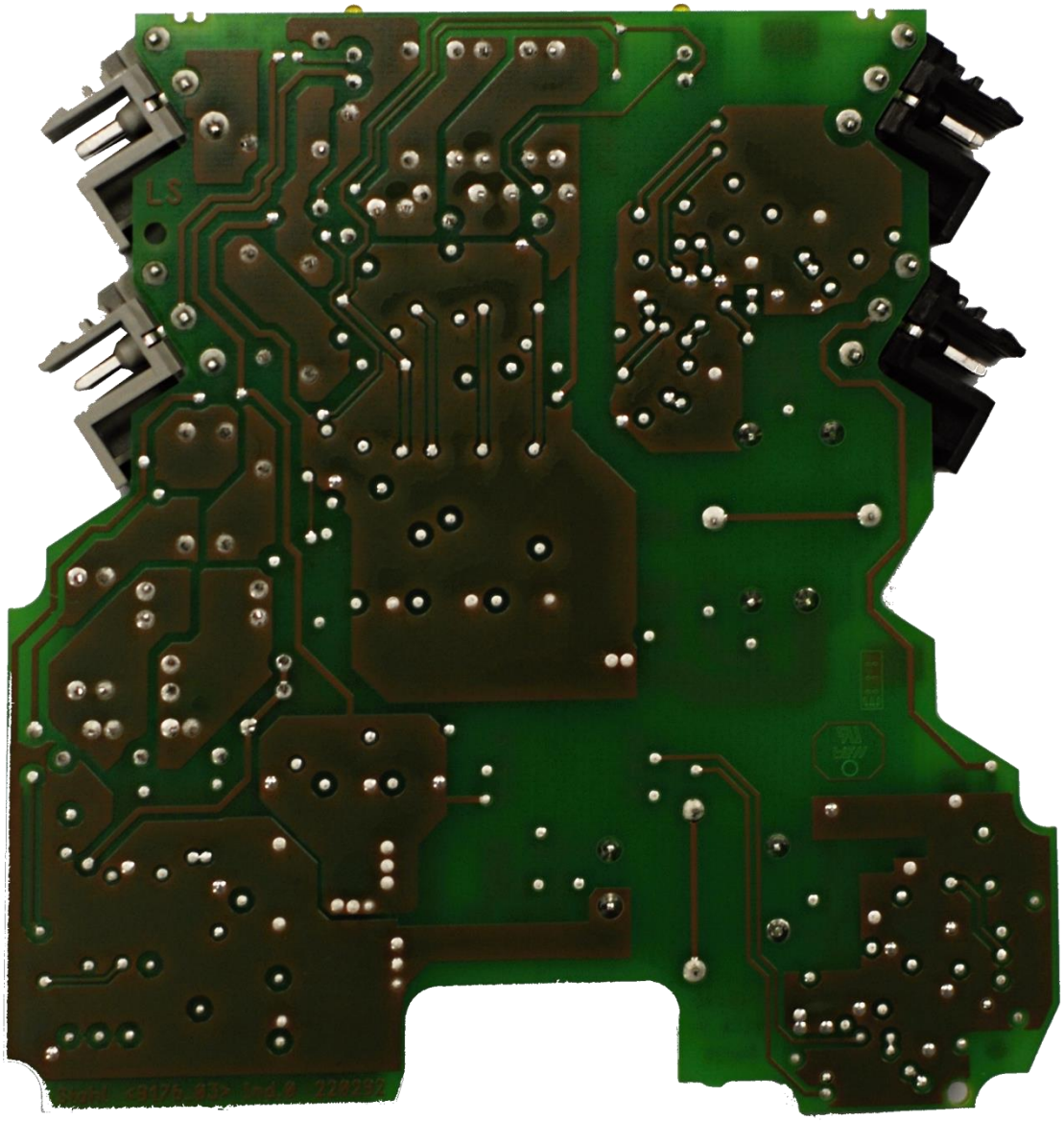
Supp. XXX Unassembled printed circuit board from top side



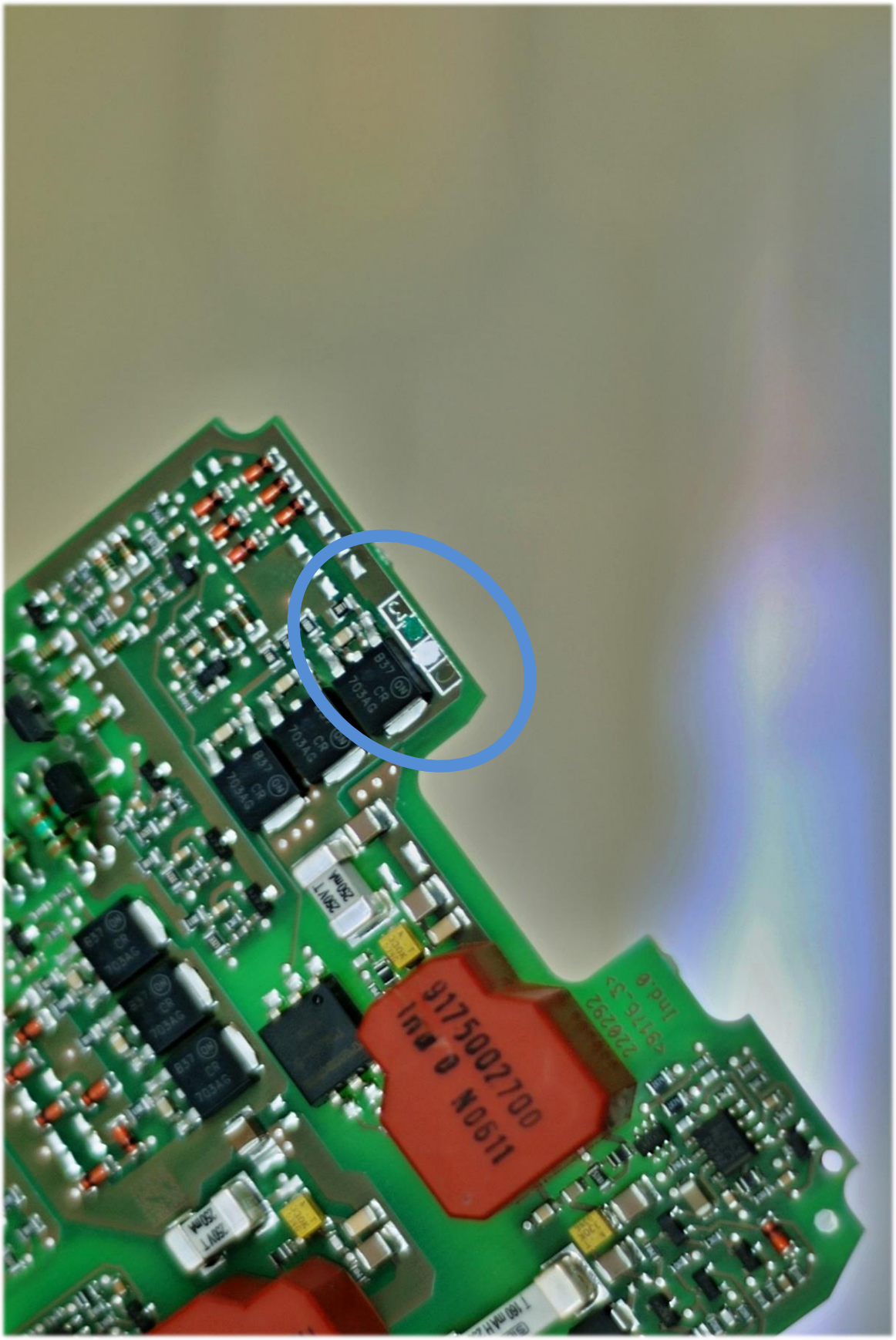
Supp. XXXI Assembled PCB – ver. 1



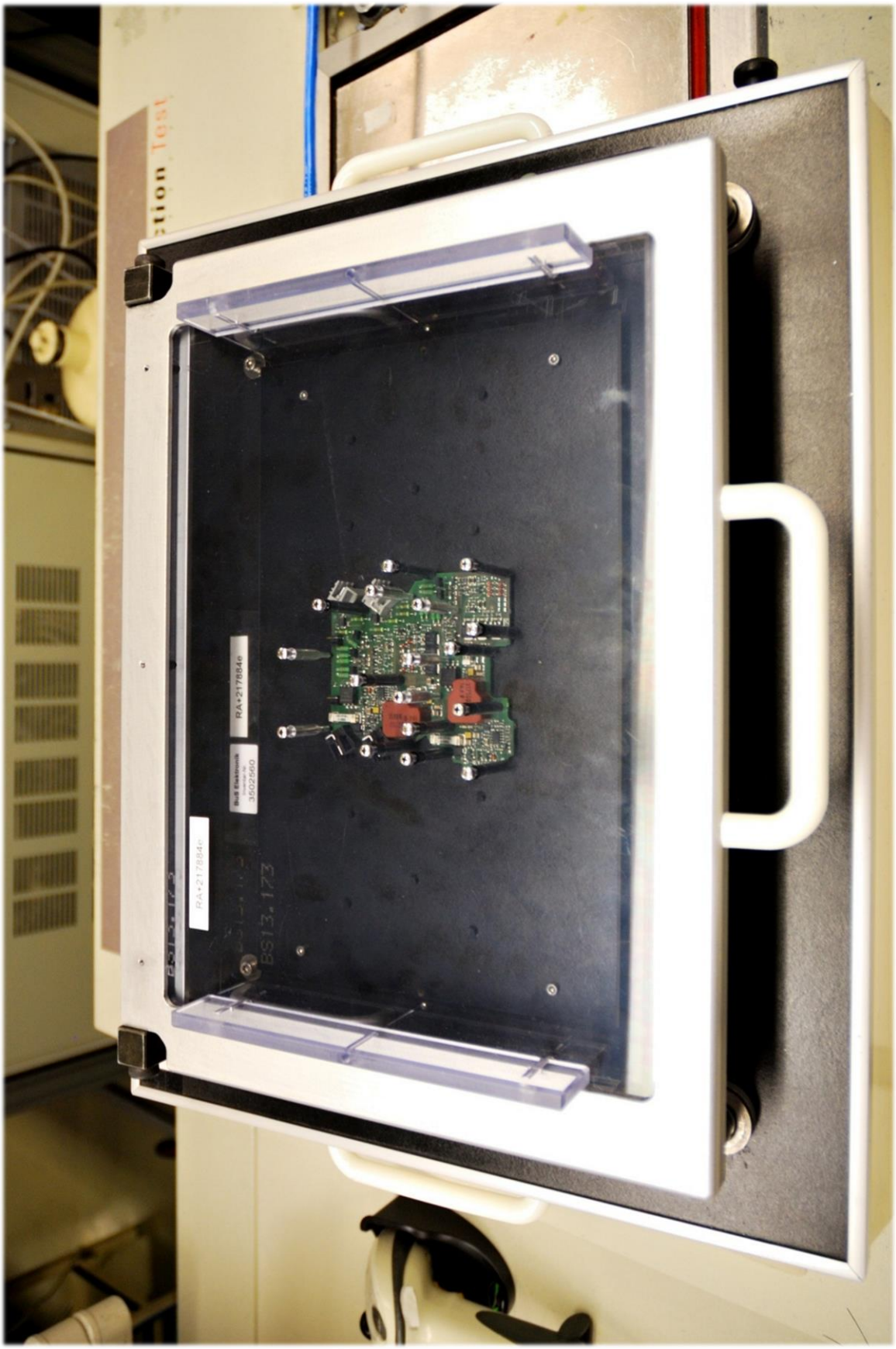
Supp. XXXII Assembled PCB – ver. 2



Supp. XXXIII Assembled PCB from bottom

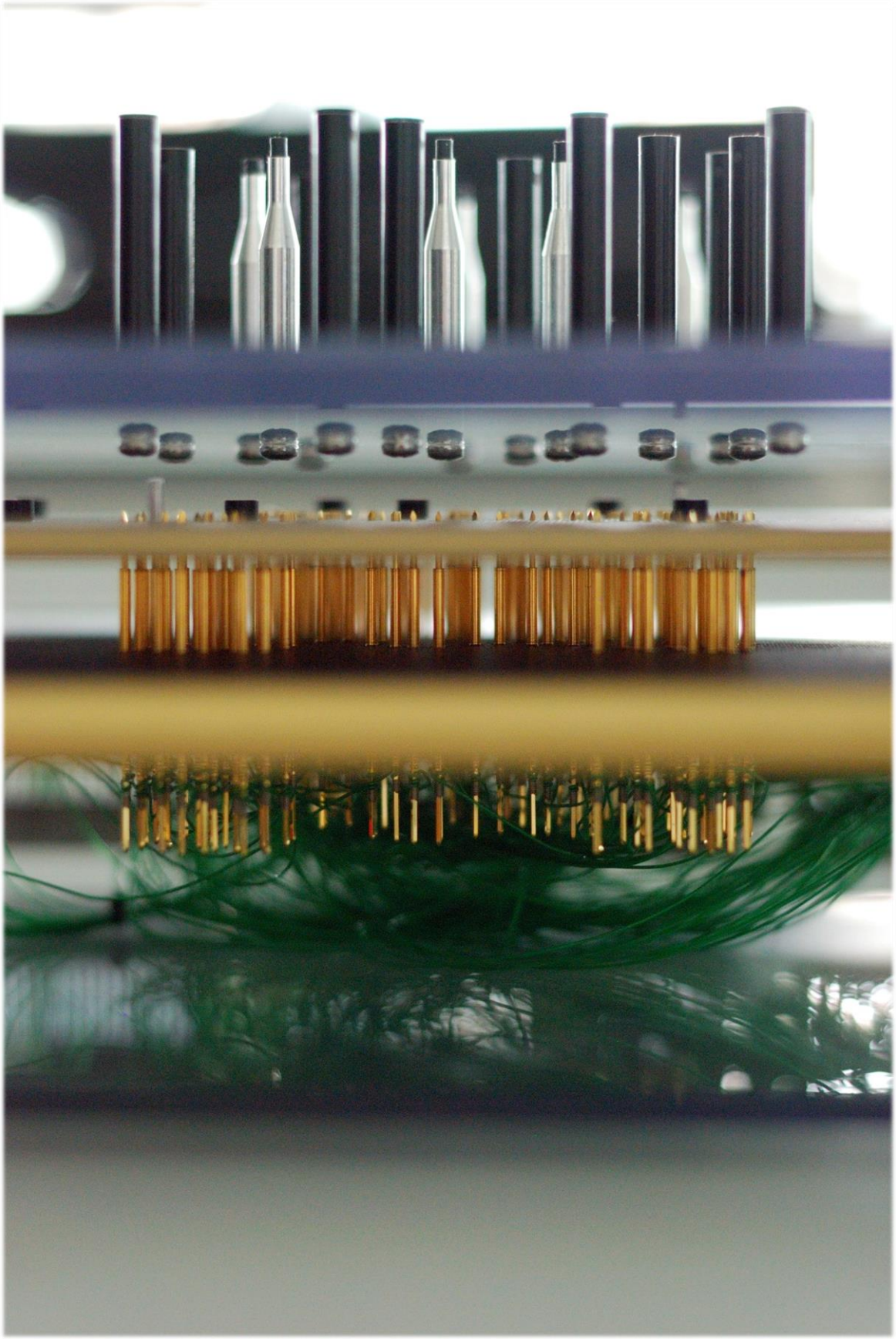


Supp. XXXIV Detail of passed point on the PCB after testing

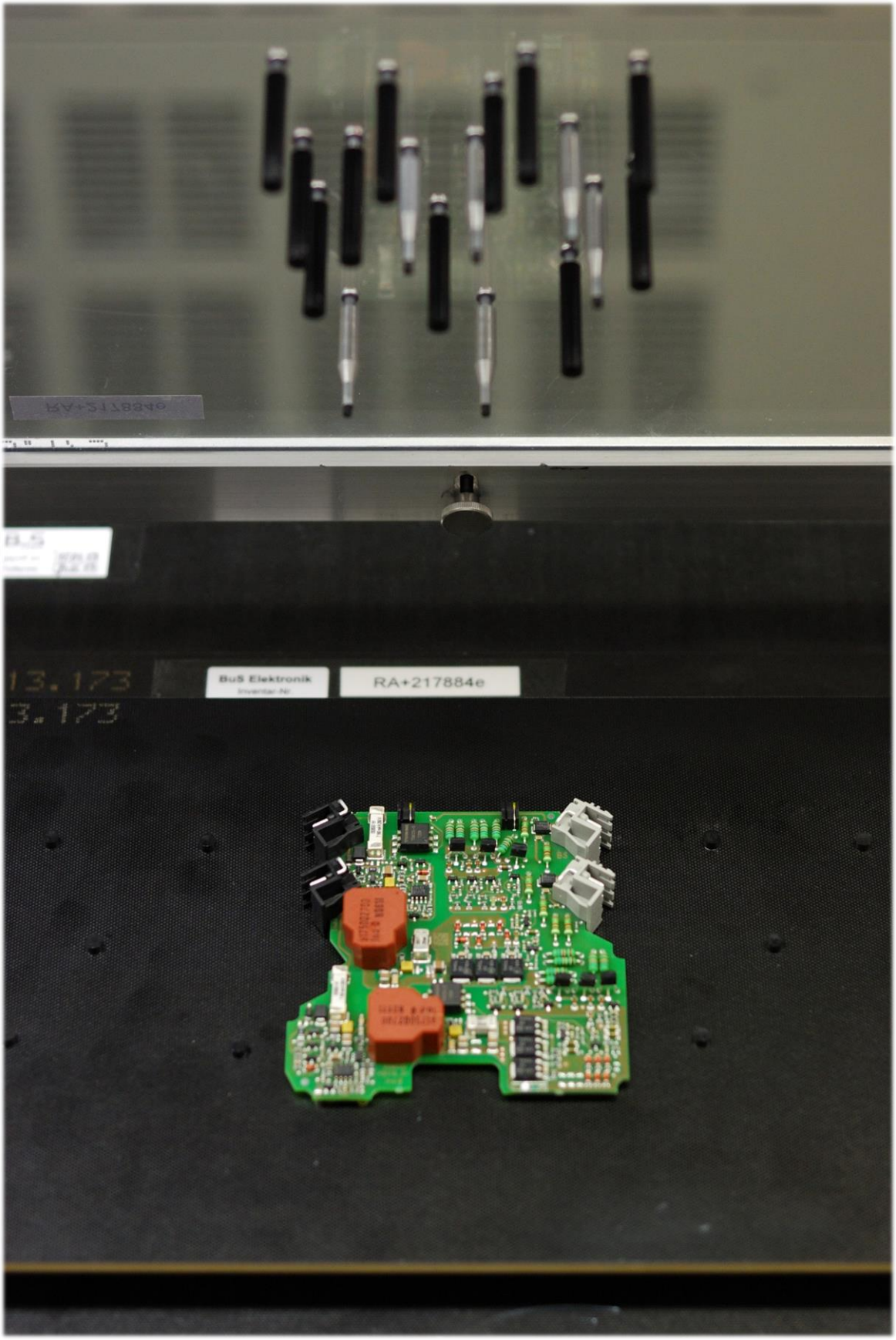


Supp. XXXV Total view at tester by testing in progress

Supp. XXXVI Inside connections and wiring of the permatech adaptor

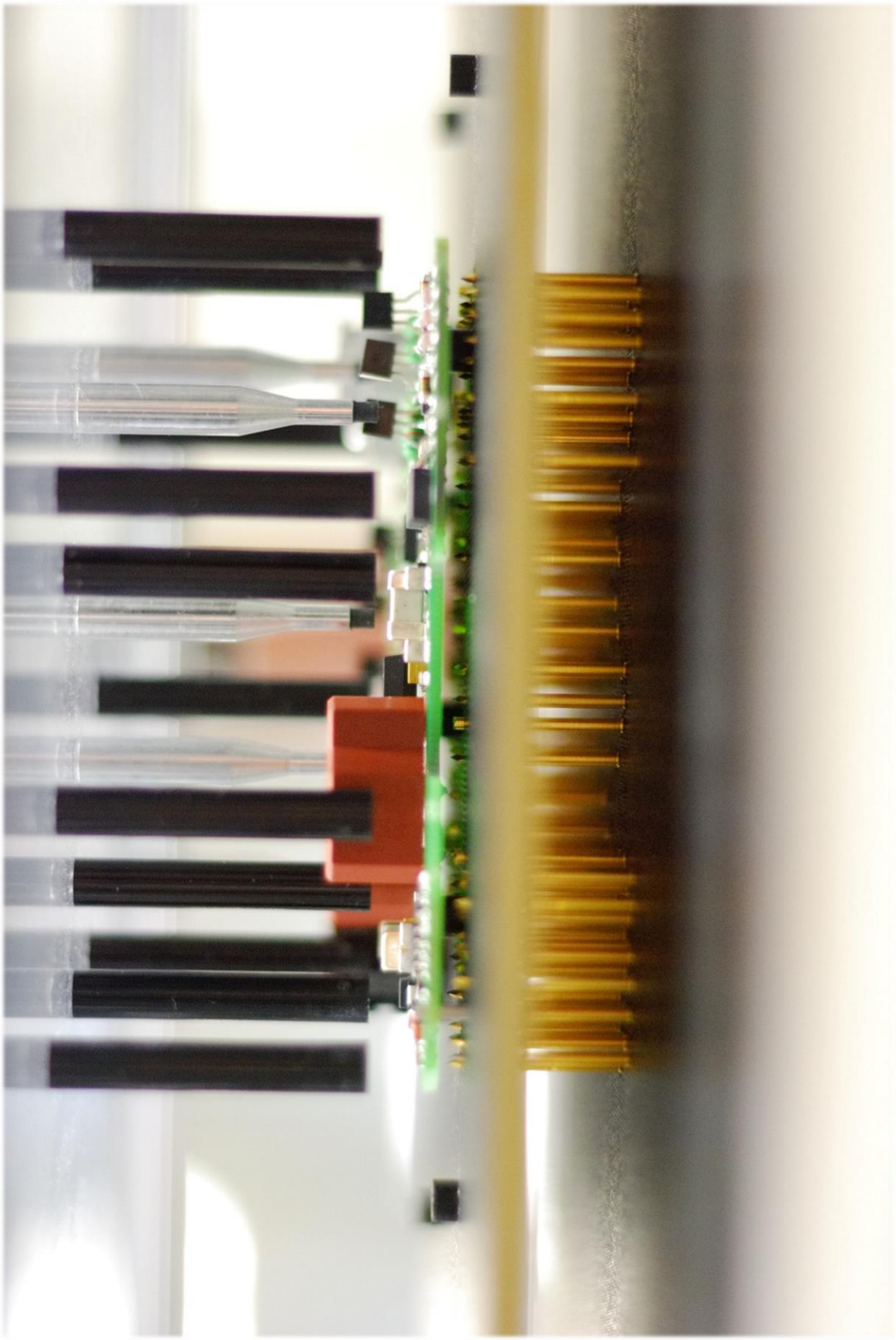


Supp. XXXVII Side sight (side cut) at fixture in transport position



Supp. XXXVIII Board placed in the fixture

Supp. XXXIX Working place with GenRad™ tester



Supp. XL Side sight at board under test with fixture lifted up

Supp. XLI Side sight at board under test with fixture pulled down